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A STUDY OF THE ELECTRICAL PROPERTIES OF P-N JUNCTIONS FORMED BY ION-IMPLANTATION INTO GALLIUM ARSENIDE

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ABSTRACT

Ion implantation in Si and Ge has been thoroughly investigated and theories are well established. One area which needs further investigation is ion-implantation in compound materials. The present work is a study of the electrical properties of p-n junctions formed by ion-implantation into GaAs and (Ga, In) As. In the process of ion-implantation, ion beams bombard the surface and create undesirable surface effects. In this study, the surface effects were investigated, and surface leakage currents were shown to be reduced by surface treatment.

Ion implantation was carried out with 10^{17} cm^{-2} In ions to convert n-type GaAs to (Ga, In)As. Subsequently 10^{14} cm^{-2} Zn ions were implanted to yield a p-n junction. For comparison, another group of n-type GaAs wafers were implanted with Zn ions only.

I-V characteristics and C-V measurements were obtained for the Zn-GaAs and Zn-(In, Ga)As junctions. The junction profiles were inferred from the I-V characteristics and the C-V measurements. The Zn-(In, Ga)As junction is considered as a p-i-n heterojunction, without generation-recombination current. The Zn-GaAs junction is considered as a p-n homojunction with appreciable generation-recombination currents.

Due to the surface effects, the electrical properties of the Zn-(In, Ga)As junctions appear to be more complex than those of the Zn-GaAs junctions. Surface treatments were carried out using NaOH and HCl to observe the effect of surface treatments on the I-V characteristic and on the reverse breakdown voltage.

ACKNOWLEDGEMENTS

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To his wife, Miaw-Shang, the author owes many thanks beyond expression for her perseverance during the strain of his study days, for providing the family income, and for taking care of their son, Dean, whose cheering smile has brightened these days of many hardships.

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1. INTRODUCTION

Ion implantation is known to be an excellent method for fabricating p-n junctions. Before the advent of ion implantation, two methods were commonly used; alloying and solid state diffusion. However, heating is an essential process in both conventional methods. Disadvantages are inherently associated with heating.

Ion implantation has been reported by Gibbons (1968) and Mayer et al. (1969) to possess several advantages when compared with conventional methods. By externally controlling the energy and the current of the ion beam, ion implantation provides a precise method in controlling doping profiles in three dimensions and in controlling precisely the amount of dopant and avoids undesirable effects resulting from thermal diffusion or high temperature alloying.

As the implanted ion slows down and comes to rest, it creates a region of heavy disorder around the ion track. Thus, ion implantation is not an equilibrium process. Annealing procedures are required to recrystallize the disorder and remove the residual strains from the crystal. Some studies indicate that annealing, if not handled properly, might develop dislocations.

Mathematical analysis of a p-n junction is usually carried out for two limiting cases: (1) the abrupt junction (2) the linearly graded junction. Physical insights are often gained by mathematical simplification. By suitably altering implantation conditions, both types of junctions can be obtained. Roughan et al. (1969) reported that a high dose and brief annealing period resulted in an abrupt junction while a

low dose and extended annealing resulted in a graded junction.

The present work is a study of the electrical characteristics of implanted p-n junctions by current-voltage measurements and capacitance-voltage measurements. I-V measurements were obtained with a semi-log simulator so that the results in this work can be compared with the commonly encountered diode characteristics. Departure from the ideal diode characteristics were analyzed. C-V measurements were used to determine whether the junction was abruptly or linearly graded. Frequency dependence of junction capacitance was also invetigated to determine whether deep level traps were present in the depletion region.

Surface treatments were also carried out on p-n junctions to observe the surface properties of the ion implanted junctions. As is well known, the surface produces only a secondary effect on the flow of holes and electrons within the bulk semiconductor provided the surface is suitably prepared. In such a case, the surface acts primarily as a physical boundary of the semiconductor crystal. However, a poor surface can destroy the desired carrier flow patterns in the bulk, and can lead to a device with useless electrical characteristics.

One of the most sensitive parameters of the surface condition is the reverse-biased current. Jonscher (1960) indicated that the surface affects the reverse current in three principal ways: (1) a grossly contaminated surface may provide a leakage path of very low resistance (2) a high generation rate at the surface increases the reverse current and may dominate it (3) the surface may have more or less abrupt catastrophic increase of current. Thus, the magnitude of reverse currents may be very sensitive to the state of the surface and to the

composition of the surrounding atmosphere. Also, the breakdown might be due either to surface breakdown or to bulk breakdown. Proper surface treatment can extend the breakdown voltage until it is limited by the bulk breakdown voltage.

The p-n junctions considered in this research work are a part of an effort to develop a practical vidicon for detecting infrared radiation. The wavelength of the infrared radiation of interest will dictate the maximum energy gap E_g of the semiconductor material in which the p-n junctions are formed by ion implantation. While the binary compound materials in general have a definite energy band gap, it is usually possible to add another element to produce a ternary compound material. The bandgap of the ternary compound material depends upon the content of the various elements in the compound material. A likely candidate for this attempt is Indium crystallized into gallium arsenide which yields an energy band gap within the range of 0.33 ev $\sim$ 1.35 ev. Epitaxially grown (In, Ga) As is technologically demanding. Ion implantation was considered as an alternative method to obtain (In, Ga) As.

P-n junctions were formed in gallium arsenide and in gallium-indium-arsenide by ion implantation. The junctions were formed by implanting zinc into each substrate material. Electrical characteristics of both types of p-n junctions were obtained. Comparison of the results indicate that while the electrical characteristics of p-n junctions formed in the gallium-indium-arsenide are more complex than the electrical characteristics of p-n junctions formed in gallium-arsenide, the primary differences are due to surface properties.

2. LITERATURE REVIEW

Research in semiconductors began early in the 1930's. Part of the early research was with crystal rectifiers undertaken in connection with the radar program during world war II and continued in several laboratories later.

In 1932, both Wilson and Nordheim independently proposed the tunnel effect as an explanation of rectification. However, their theories did not gain support at the time.

The importance of minority carriers in determining the rectifying action was first pointed out by Davydov (1938) of the USSR. The concepts of nonequilibrium density and finite lifetime of carriers was also included. However, prior to 1949, the general view of rectification was that p-type and n-type semiconductors were "boxes" of Maxwell-Boltzmann gases of electrons and holes with a potential barrier at the p-n boundaries. This theory of rectifying action gives the right qualitative result of an exponential law for rectification but the quantitative theory for the properties of semiconductors was first introduced by Shockley (1949).

Shockley (1949) treated the p-n junction diode as consisting of three regions, an infinitely long p-type region, a barrier region and an infinitely long n-type region, and derived the so called "ideal current-voltage characteristics" based on the rate of diffusion and recombination of minority carriers. This derivation was based on four assumptions: (1) an abrupt depletion layer (2) the Boltzmann approximation (3) low injection and (4) the absence of generation currents in the

depletion layer. Since few diodes meet those requirements, it was found that ideal current-voltage characteristics were limited to germanium at low current and was not applicable in the case of silicon at room temperature. While the departure from ideal was inevitable, the simple theory of Shockley has served as a basis for many extensions and modifications.

It was observed that departure from ideal is in the direction of poor rectification, and forward characteristics are of the form $I \propto \exp(e\,v / n\,k\,T)$ where $n = 1 \sim 2$ at low injection levels. The departure from an ideal current may be in part accounted for by a recombination and generation current. The complete treatment was given by Sah et al. (1957).

Surface effects are also known to cause departure from ideal. Shockley (1950) indicated that the recombination rate of holes and electrons at the surface can be changed by surface treatment. Brattain et al. (1953) found that the properties of the germanium surface can be changed by exposing the surface to various gases and chemicals and that the surface can be cycled back and forth between two extremes of small or large surface dipole layers of charge.

The existence of inversion layers which contribute to leakage current was reported by Brown (1953) in his study of n-type surface conductivity on p-type germanium. Based on this, Cutler et al. (1954) developed a simple model to account for leakage current in rectifiers which showed good agreement with experiments.

Ericksen et al. (1957), in their investigation of excess currents on silicon and germanium diodes, reported that inversion layers give an

approximate logarithmic increase of excess currents with applied voltage.

In their review of surface properties of semiconductors, Brattain et al. (1954) regarded the surface pictorially as a discrete semiconducting phase, and suggested that their properties may be changed by altering the chemical nature of the surface. Gases interact with the surface by exchanging charge with the semiconductor. For anodic bias, the important reaction is $X^- + p \rightleftarrows X$ and likewise for cathodic bias $Y^+ + n \rightleftarrows Y$. ($X^-$ and Y^+ represent ionized gases.)

It follows that in the germanium surface - gas interaction, the dissociation of O_2 on the germanium surface is governed by the reaction $O = O^- + p$, and in the water vapor interaction, H_2O may dissociate on the surface by $H_2O \rightleftarrows OH^- + H^+$. However, just what role the electron (n) plays in this case or why it is the electron instead of the hole (p) remains unexplained.

Kingston (1956) distinguished two types of surface states. The "fast" states have a hole or electron capture time not greater than a microsecond and are chiefly involved in the recombination process. The "slow" states have a capture time from a millisecond to several minutes and determine the density and types of carriers at the surface. "Fast" states are believed to occur at the interface between the semiconductor and oxide layer. "Slow" states are associated with the structure of the oxide layer and the ambient gases.

It is also well known that the reverse saturation current is very sensitive to the surface conditions. In his study of the correlation of I-V characteristics with noise, Monteith (1963) observed that the

reverse saturation currents and noise were correlated in different ways for different surface treatments. Relating to the present work, one expects that optimum reverse saturation current can be obtained by proper surface treatment.

Much work has been done on silicon and germanium. It remains to be seen how the theory developed and experimental results obtained may be extrapolated to other semiconducting materials. One of the areas of current interest is compound semiconducting materials. The first comprehensive review of compound semiconductor was given by Jenny (1958).

Due to its reasonably wide band gap, gallium arsenide has been considered as the most prominent compound semiconducting material which might find application at high temperatures.

The most commonly used p-type dopant in GaAs is Zn. It has been reported by Ermanis et al. (1966) that the predominant Zn species in GaAs is a Zn atom on a substitutional Ga lattice site which behaves as a singly charged acceptor with a small ionization energy. He remarked that the ionization energy of Zn in GaAs was given by Meyerhofer to be 0.014 ev, which did not appear to depend on the concentration in the range of $2 \sim 7 \times 10^{17}$ cm^{-3}.

3. EXPERIMENTAL

3.1. Preparation of Samples

3.1.1. Introduction

The ion implantations of n-type GaAs were carried out at Langley Research Center.

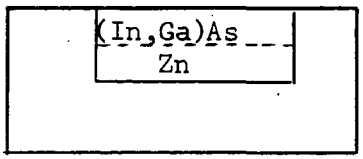
The samples were received from NASA and the subsequent annealing, making ohmic contacts and encapsulation were done in the Semiconductor Device Laboratory at North Carolina State University.

The resistivity of n-type GaAs wafers before implantation was 0.04 ohm-cm with a background concentration of 5×10^{16} cm^{-3}. Ion implantation was carried out with 10^{17} cm^{-2} In ions to convert the implanted region to (Ga, In) As. Subsequently 10^{14} cm^{-2} Zn ions were implanted to yield a p-n junction. For comparison, another group of GaAs wafers were implanted with Zn ions only. Figure 3.1. schematically depicts the profile of ion-implanted samples for both groups of samples.

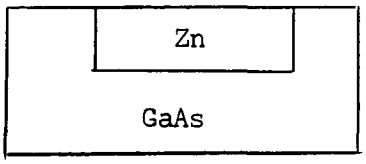
Table 3.1. Ion implantation data

Wafers n-type GaAs Nd = 5×10^{16} cm^{-3}	Dopant	Dosage (cm^{-2})	Beam Energies (kev)	Beam	Temp.
I	Indium	10^{17}	60	spot	220°F
	Zinc	10^{14}	60	scan	Room T.
II	Zinc	10^{14}	60	scan	Room T.

For the purpose of identification, and to subject each sample to different annealing conditions, the wafers were sliced as shown in Figure 3.2. and labeled accordingly.



(1)



(2)

Figure 3.1. Cross-sectional drawings of ion implanted junction devices for (1) Zn- (In, Ga) As and (2) Zn-GaAs

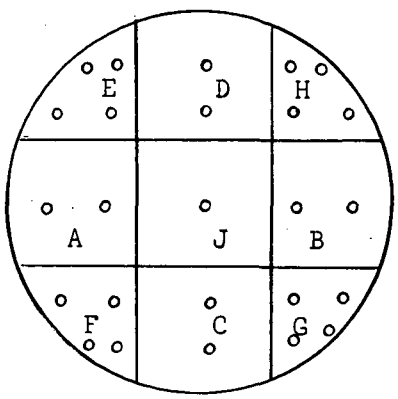


Figure 3.2. Schematic diagram showing locations of each sliced sample

3.1.2. Fabrication

Before slicing, the wafers were coated with spin-on Si O_2 (Emulsitone*) (3500 rpm for 15 sec) followed by baking at 200°C for 10 min to prevent outdiffusion of Zn.

Annealing As noted earlier, annealing is necessary to reduce disorder and bring about realignment of atoms inside the material (Ref. Marsh et al. (1967)). The samples were annealed in N_2 ambient and at temperatures of 400°C, 600°C and 800°C respectively. The details are listed in Table 3.2.

Table 3.2. The annealing conditions for each sample

Samples	Annealing Temp. (C)	Annealing Time (min.)	Ambient Gas
ID	600	30	N_2
IE	600	30	N_2
IF	600	30	N_2
IG	800	30	N_2
IH	400	30	N_2
IIA, B	400	30	N_2
IIE, F, G, H	600	30	N_2
IID, C	800	30	N_2

Making ohmic contact Si O_2 was first removed from the back surface by dipping in (2/1) HF solutions (water: 50% HF) for 1 minute.

*Trade name

Wafers were then fixed to glass plates and Si 0_2 removed from the back surface by sand blasting. Then each was dipped in HF (1:1) again to remove any Si 0_2 left. After rinsing in deionized water and drying in N_2, the plate was removed. After masking with wax, gold and tin were electroless plated on the backsurface. The back contact usually required several attempts before Au-Sn alloy contact was formed. The samples were heated on a strip heater at about 300°C - 310°C until the surface became shiny. Gold dots of 750°A to 1000°A thickness were then evaporated onto the implanted regions. A contact resistance less than 100 ohm was acceptable.

Encapsulation. The devices were mounted on TO-5 headers, electrical contacts achieved with bonded gold wires and finally encapsulated.

3.2. Current-Voltage Characteristics

The equipment used in taking the current-voltage characteristics included a logarithmic curve tracer and an X-Y recorder. The logarithmic curve tracer records the linear input voltage and the log of output current on chart paper.

Logarithmic curve tracer In the study of diode characteristics, a knowledge of voltage-current characteristics over a wide range of currents is needed. The curve has to be continuous so that changes in the slope are recorded. The diode current is known to be an exponential function of the diode voltage (there are exceptions, i.e. some follow power law), a wide range is available using a logarithmic current scale and a linear voltage scale.

The schematic diagram of the curve tracer is shown in Figure 3.3. In order to obtain a voltage, V, proportional to log I, a transconductor is connected between the output and inverting input of a high-gain operational amplifier as shown in the same figure. The amplifier is chosen for low offset voltage, low offset current, and low drift. The transconductor may be either a diode or a transistor connected as a diode (base and collector common) or a transistor connected as shown. It must have a voltage which is proportional to log I over a wide current range.

X-Y Recorder A Hewlett-Packard 7035B X-Y recorder was used. The scale has been set so that the current can be varied from 10^{-2} to 10^{-9} amp and the applied voltage can be varied from 0 to 10 volts for reverse bias and 0 to 1 volt on the expanded scale for forward bias.

Procedures Since the technique of taking current-voltage characteristics is well known, only a brief and somewhat general description will be given.

Calibration was first made using a standard current and voltage source provided in the logarithmic curve tracer. The scan rate was set moderately slow so that movement along the current axis will track the rate of linear voltage increase.

Because a window opening was purposely made in the device housing, the device was extremely sensitive to light. An opaque cap was substituted to exclude light during the curve tracing.

Instability resulting from excess charge accumulation seemed to predominate during the initial stage of curve tracing. It takes sometime before stability is regained and normal functioning restored.

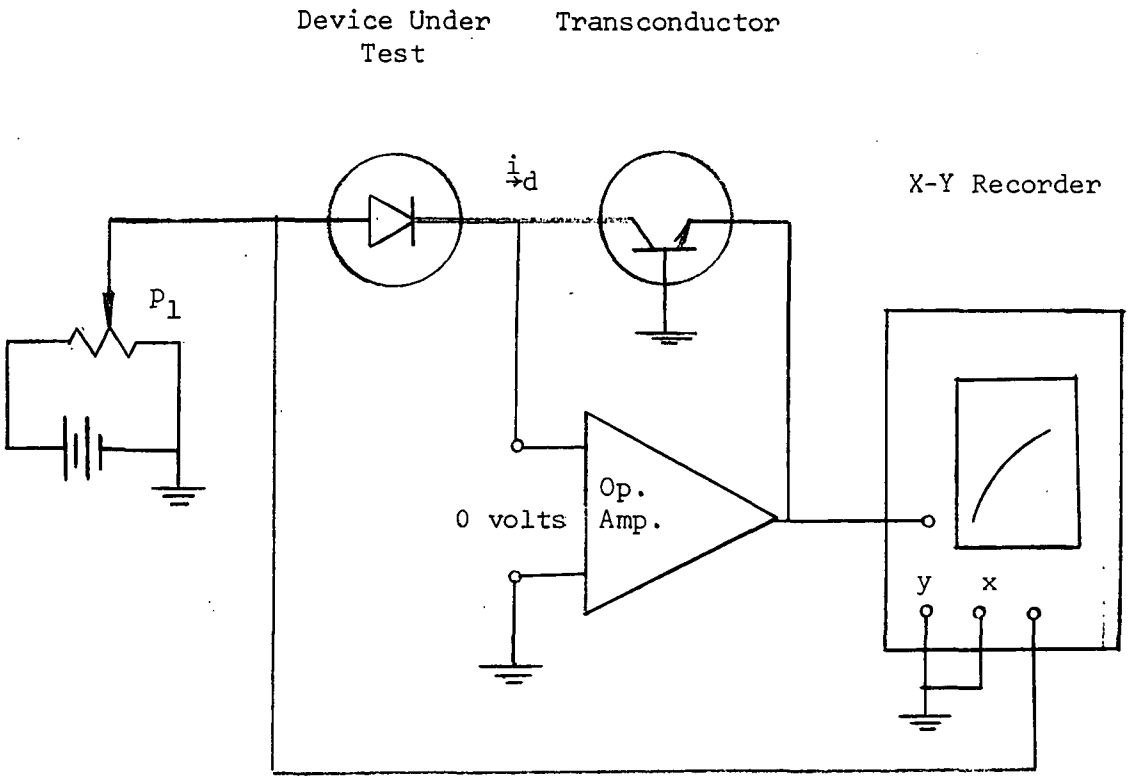


Figure 3.3. Schematic diagram of logarithmic curve tracer using operational amplifiers

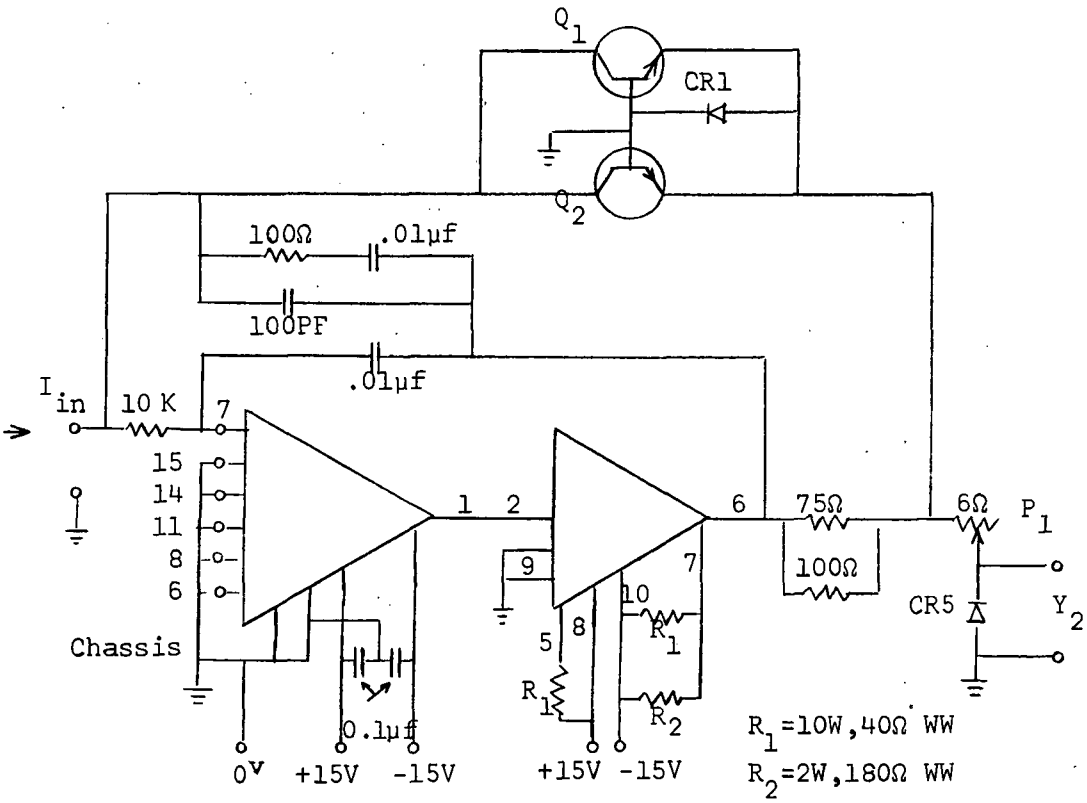


Figure 3.4. Details of log conversion circuit (after operation manual)

Repeatability was found to be within an acceptable range.

3.3. Capacitance-Voltage Measurement and Its Frequency Dependence

C-V measurement An automatic display system was first thought to be a desirable instrument to take the C-V measurement. However, the devices were found to be too leaky to be measured automatically so that the possibility of using automatic display system was ruled out. The next choice is of course a point-by-point measurement using the capacitance bridge.

Figure 3.5. shows the block diagram of the system used. The system is basically a standard impedance bridge with auxiliary equipment to provide and measure the bias voltage. The impedance bridge was type 1608-A impedance bridge by General Radio Co.

The capacitance bridge as well as the method for applying bias is shown schematically in Figure 3.6. Since the bridge and the dc supply do not have a common ground, one must be left floating. Also due to high D (dissipation factor), the bridge selector was set to C_p instead of C_s.

The accuracy of the capacitance reading is given to be ± 0.1% of the reading ± 0.005% of full scale (±1/2 of the last digit) for the frequency range 20 cps - 20 KC.

Measurements are tabulated and the curves plotted for $1 / C^2$ or $1 / C^3$ in chapter 5.

Frequency dependence of C-V measurement The purpose of this experiment was to determine if the junction capacitance decreases with increasing frequency. If that is the case, the presence of defect

Wide Range Osc.

Model 200CD (HP)

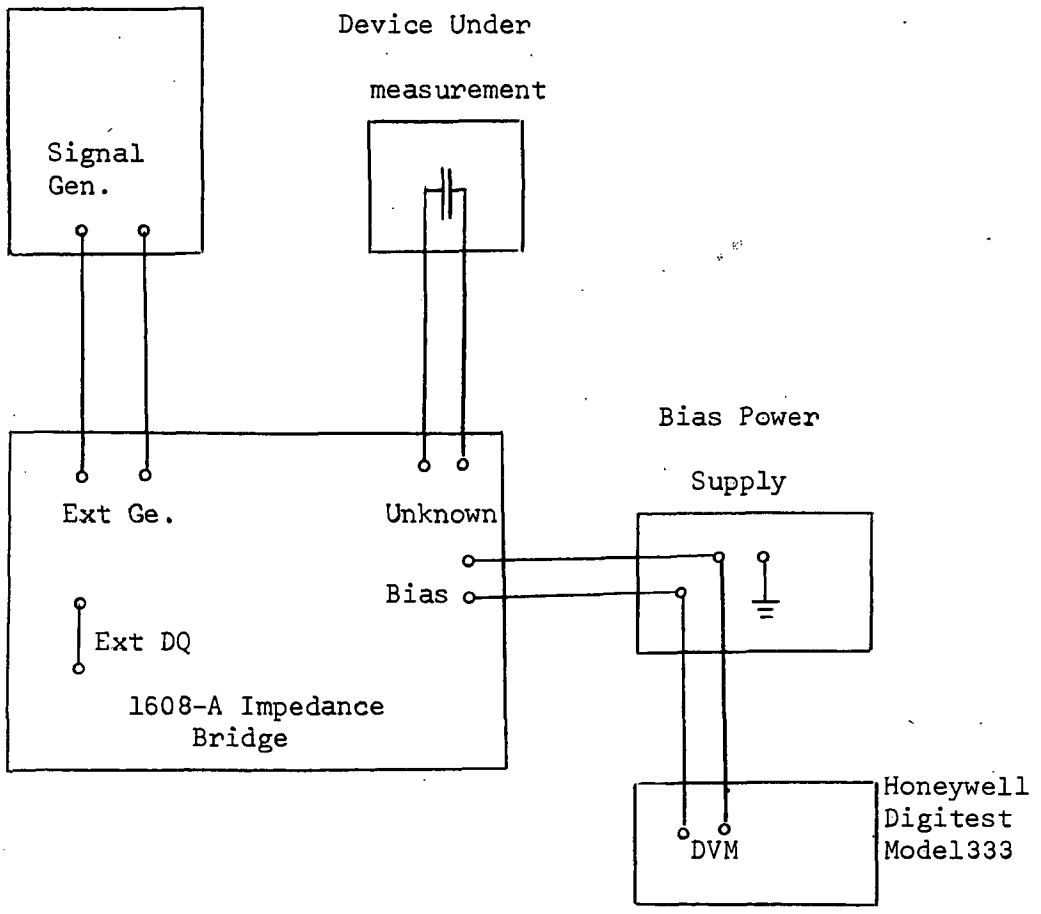


Figure 3.5. Sketch of C-V measurement and its frequency dependence

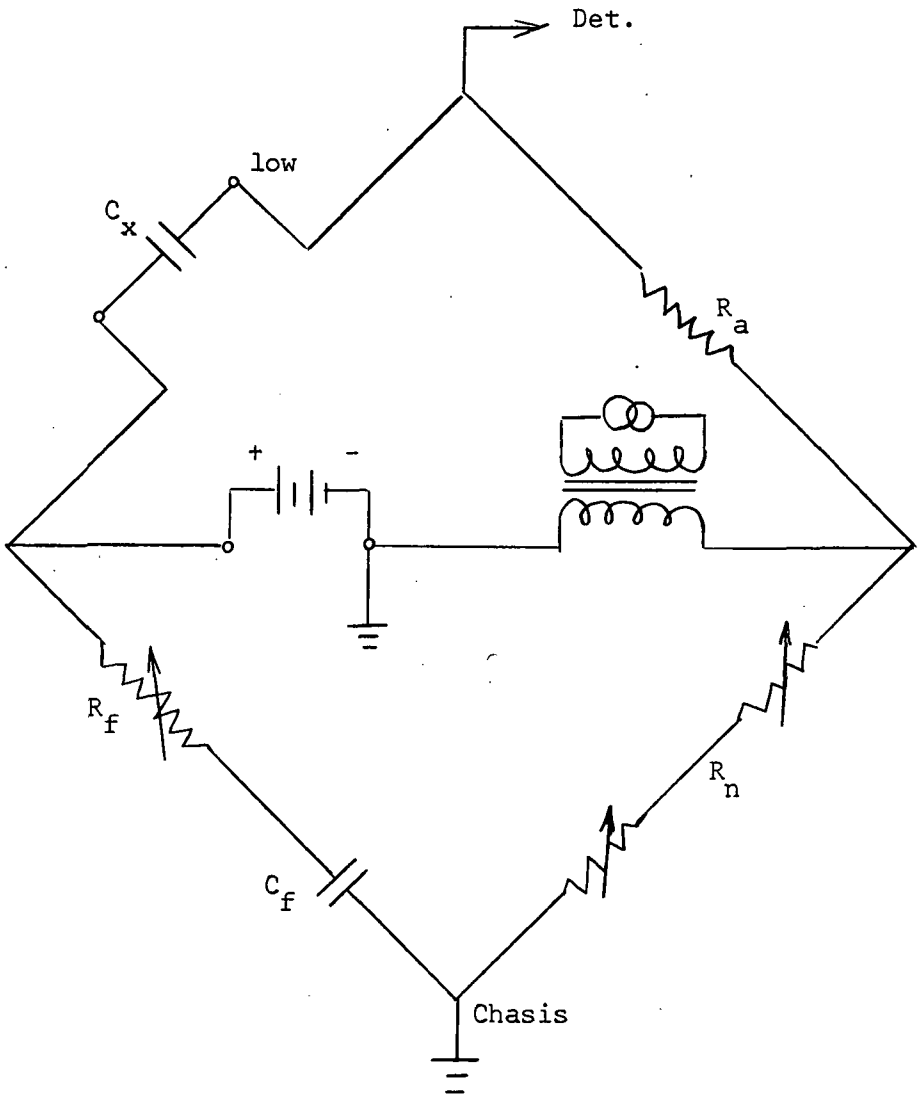


Figure 3.6. Schematic diagram of impedance bridge showing method of applying dc bias to capacitor

trapping centers can be predicted.

The equipment used in the capacitance-voltage measurement is adequate to perform this experiment. However, since the 1608A impedance bridge only provides a 1 KC internal oscillator, a signal generator providing a range of frequencies had to be connected externally.

3.4 Surface Treatments

Surface treatment with various gases and chemicals have been widely used to change the surface properties. The change in surface properties can be measured either by contact potential as suggested by Brattain et al. (1953) or by channel conductance as described by Buck et al. (1958). The surface treatment could also be used to change noise output and the I-V characteristics.

In this section, a method for changing the I-V characteristic and reverse breakdown voltage using surface treatments will be described.

Since the initial surface conditions are never fully understood, we assumed that the surfaces were p-type and attempted to change from a p-type to an n-type surface. This assumption is plausible, since it is believed that the periodic crystal lattice suffers an abrupt discontinuity at the surface, and the dangling valancy has a tendency to capture or rather "accept" electrons, therefore the surface is in general believed to be p-type.

As a first step in this endeavor, exposure of the surface to various chemicals (acids, bases, etc.) and cycling the ambient gases were tried. Combined effects were first observed and recorded.

Surface treatment (5/1) Hydrochrolic Acid (HCl): Deionized water was used. First the specimen was removed from the header and dipped into the solution. The dipping time varied from a few seconds to 30 min. depending on the observed changes. The specimen was then removed from the solution and washed in running deionized water for 10 sec to 20 sec. Then it was dried in dry purified N_2. The specimen was enclosed in a chamber flushed by various gases and I-V characteristics recorded.

Gas Chamber Figure 3.7. shows the schematic diagram of the set-up. The outlet of purified N_2 was connected by acetate tubing to a flask half filled with deionized water and N_2 was allowed to bubble through the water. The wet N_2 was then fed into the chamber.

After the surface of the device was treated and the device mounted in the chamber, I-V characteristics were recorded. The process was continued if the I-V characteristics showed improvement. The improvement was defined by a decrease in reverse saturation current and by the forward current approaching ideal characteristics as predicted by Shockley. Both the dipping time and concentration of the solution were varied as the I-V characteristics improved.

During the process of dipping in the solution, the back contact as well as the gold dot on the implanted area were etched. Therefore, the devices were checked for ohmic contact before each run was attempted.

When the point was reached where the reverse saturation current started increasing again, the solution was switched to sodium hydroxide (NaOH). This solution is believed to change an n-type surface in the direction of p-type surface.

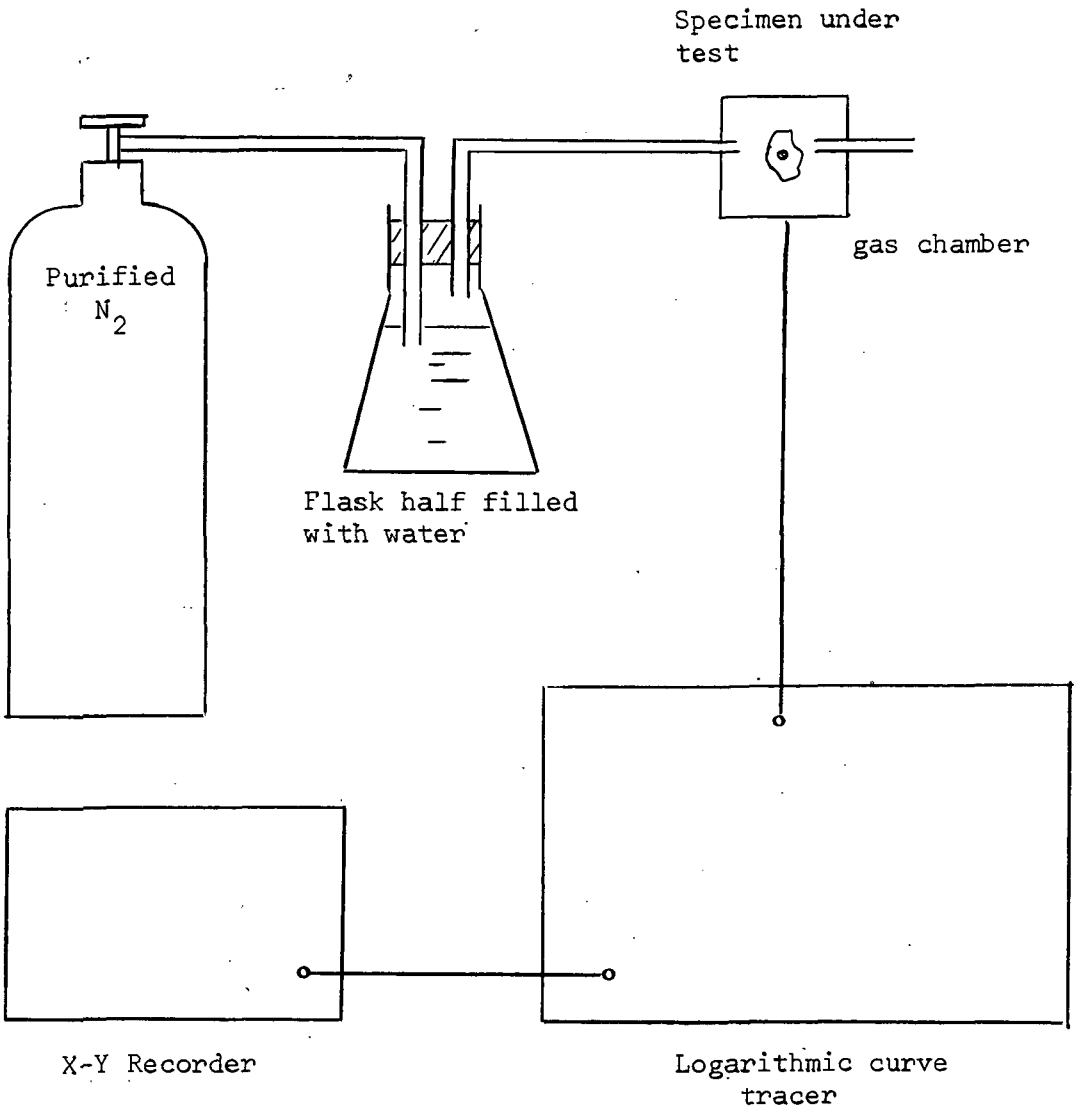


Figure 3.7. Schematic diagram showing the equipment used to measure I-V characteristics of the devices with the surface exposed to various gases.

After several trials, it was decided that gases had little effect on changing the surface properties, so that the gas chamber was totally discarded. By confining the variables to a single parameter, the correlation between surface treatment and I-V characteristics is simplified.

Surface treatments were carried out to investigate their effect on the breakdown voltage. Since inversion layers formed on the surface provide leaky channels and thus reduce the breakdown, it can be expected that by reducing the inversion layer, breakdown can be postponed until it is limited by the bulk breakdown.

Samples were picked at random. Surface treatments were applied to I-E-1 and II-E'-1. Solution (5/1) NaOH: Deionized water was used. Dipping times were 20 min., 60 min. and 40 min. Pictures of the I-V characteristic of the devices including breakdown were taken with a polaroid camera (Tektronix Elgeet 3" F 1.9).

4. THEORY

4.1. P-N Junction and Capacitance-Voltage Characteristics

4.1.1. General

A p-n junction is generally described as a transition from p- to n-type regions within a semiconductor lattice. The rate of transition from p- to n-type may be abrupt or gradual depending on the technique used to form the junction as was briefly mentioned in chapter 1. However, to posses some degree of rectifying action, some sort of abruptness has to be assumed.

When both p- and n-type crystals come into contact, diffusion of electrons to the p-type and holes to the n-type crystal takes place due to the density gradient for both carriers. This results in a depleted region, where one observes a negative space charge in the p-region and a positive space charge in the n-region due to immobile impurity atoms. This space charge results in an electric field which opposes the flow of diffusion currents. Equilibrium is reached when both electron and hole currents are zero (i.e. the diffusion and drift components are equal and opposite). These consequences are shown in Figure 4.1. Here for simplicity, we assume the abrupt junction and $N_d > N_a$ (where N_d denotes donor impurity density and N_a, acceptor impurity density) for impurity concentration. Diagram (b) shows the energy band structure. For illustration, a homojunction is assumed; a heterojunction will be treated later. Since the general principle is that the Fermi energy is constant throughout the system in thermal equilibrium (i.e. in the absence of externally applied fields, temper-

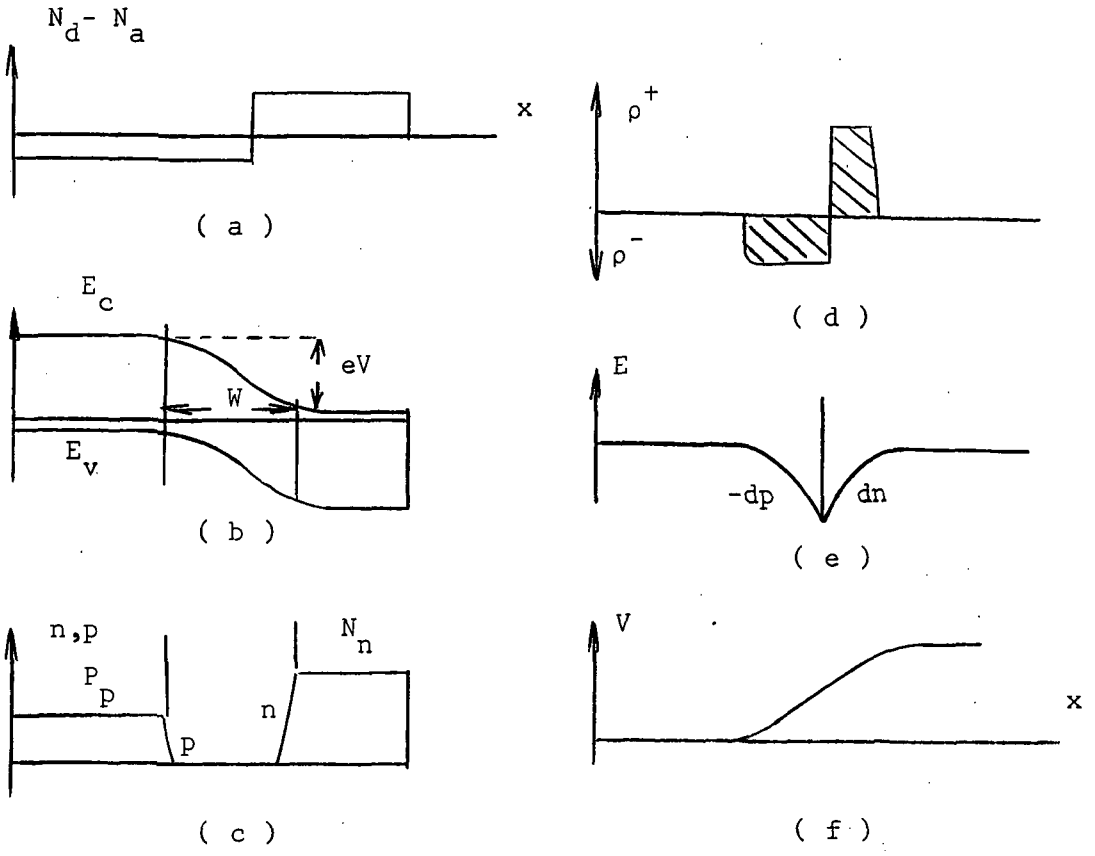


Figure 4.1. The one-dimensional abrupt p-n junction in equilibrium
(a) impurity concentration (b) energy band structure
(c) electron and hole concentration (d) net charge density
(e) electric field (f) electrostatic potential

ature gradients and external exitations etc.) some bending of the band structure is needed to take into account the fact that the Fermi level E_f is near the valence band in p-type and near conduction band in n-type material. What we obtained is a flat band on both ends with bent bands in between to account for space charge in the region. By the assumption $N_d > N_a$, the majority carriers are specified such that $n_n > p_p$. It can be shown that $d_p N_a = d_n N_d$ (where d_p denotes the depletion length of p type material and d_n, the depletion length of n type material) so that charge neutrality can be maintained. Both shaded areas are therefore equal. Diagram (e) depicts the electric field over the space charge region. The maximum electric field occurs at the junction. The electric field is obtained by Poisson's equation (which is a special form of Maxwell's equation) as

$$\nabla^2 V = - \nabla . E = - \frac{q}{\varepsilon} (p - n + N_d - N_a) \qquad (4.1.)$$

where q is the magnitude of electronic charge, P the hole concentration and n the electron concentration. By integrating the above equation once, we can obtain the electric field E, and twice to get electrostatic potential V, which is the built-in potential due to space charge. At the same time, the carrier densities n (electron) and p (hole) are related to the potential V by Boltzmann's equation:

$$\psi = \frac{q V}{k T} = \ln \left(\frac{n}{n_i}\right) = - \ln \left(\frac{p}{n_i}\right) \qquad (4.2.)$$

where n_i is the intrinsic carrier concentration.

Equations (4.1.) and (4.2.) may be regarded as a set of three equations to determine three unknowns n, p and V or ψ.

Thus, when p- and n-type semiconductors form a p-n junction, a very important property results: There is a space charge and an electric field across the junction creating a built-in potential across the junction even in thermal equilibrium. The built-in potential V_{bi} is dependent on the doping level and can be calculated by substituting appropriate boundary conditions to obtain

$$V_{bi} = V(d_n) - V(-d_p) = \frac{q}{2\varepsilon}(N_a d_p^2 + N_d d_n^2) \qquad (4.3.)$$

where d_p and d_n are the depletion length into p- and n-type material respectively and ε the dielectric constant of the material.

4.1.2. Capacitance-Voltage Characteristics

The capacitance of a parallel plate is given by

$$C = \frac{a}{d}\varepsilon \qquad (4.4.)$$

where a is the area of the plate, d the separation of the plate, ε the dielectric constant of the material.

By the same token, the p-n junction capacitance can be regarded as a parallel plate capacitor where the distance between the plates is just the depletion region width $d_p + d_n$.

Because of this simple relation between the reverse-bias junction capacitance and the depletion length, measurement of junction capacitance will provide a very convenient way to characterize the impurity distribution.

Depletion width The depletion width of the junction W is given by

$$W = d_p + d_n. \qquad (4.5.)$$

Both d_p and d_n are dependent on the applied bias as well as the impurity concentration.

For the abrupt junction, it can be shown (see Appendix 9.1.) that

$$W = \{\frac{2 \varepsilon V_{bi}}{q} (\frac{N_a + N_d}{N_a N_d})\}^{1/2} \qquad (4.6.)$$

For a linearly graded junction, we assume

$$N_d - N_a = g x$$

where g = the gradient of impurity concentration in cm^{-4} and obtain

$$W = \{\frac{12 \varepsilon}{q g} (V_{bi} - \frac{2kT}{q})\}^{1/3} . \qquad (4.7.)$$

C-V Characteristics Thus far, we have derived the depletion width under thermal equilibrium. Now, by applying external bias, readjustment of d_n and d_p is required. This is accomplished by essentially instantaneous movement of majority carriers into (or out of) the transition region. A change in d_p and d_n also implies a change in the stored charge. Thus, this charge must be moved into or out of the region to accommodate a change in junction voltage. Therefore, we must associate a capacitance with the transition region.

Depletion width changes with changes in $(V_{bi} \pm V_a)$ where $\pm$ signs are for the reverse and forward applied bias conditions respectively. Thus, for an abrupt junction

$$W = \{\frac{2 \varepsilon(V_{bi} \pm V_a)}{q} (\frac{N_a + N_d}{N_a N_d})\}^{1/2} \qquad (4.8.)$$

and for a linearly graded junction

$$W = \{\frac{12\varepsilon}{qg} (V_{bi} - \frac{2kT}{q} \pm V_a)\}^{1/3} \qquad (4.9.)$$

By definition, the capacitance of the depletion layer is given by

$$C = \frac{d\,Q}{d\,V} . \qquad (4.10.)$$

This is a general definition of capacitance even if Q is a non-linear function of V.

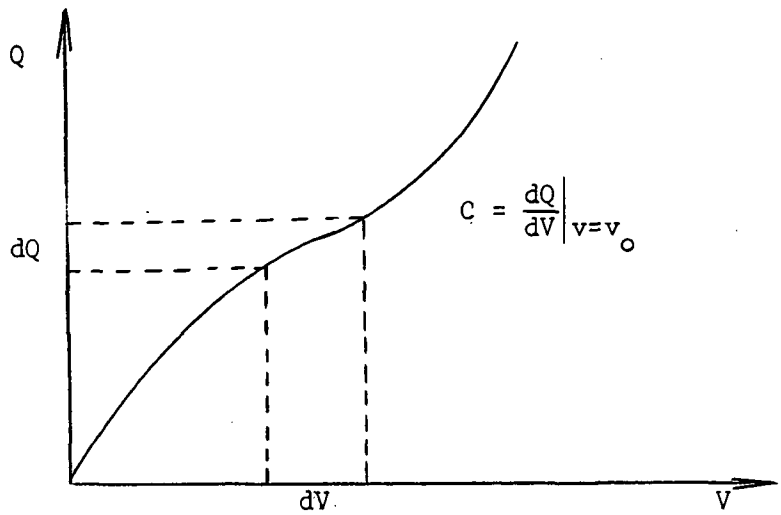


Figure 4.2. Non-linear C-V curves illustrating the general definition of capacitance

As is usual in a p-n junction, one side is more heavily doped than the other. The depletion region will be mainly extended into the lightly doped side and the charge concentration can be approximated by one type of impurity. Thus, for an abrupt junction, we have

$$Q = q\,N_a\,W \qquad \text{(assuming } p^+\text{- n junction)} \qquad (4.11.)$$

$$V = \frac{q\,N_a}{2\,\epsilon}\,W^2 . \qquad (4.12.)$$

Then,

$$C = \frac{dQ}{dV} = \frac{\frac{\partial}{\partial W}(qN_aW)\,dw}{\frac{\partial}{\partial W}(qN_aW^2/2\varepsilon)dw} = \frac{q\,N_a}{q\,N_a\,(2W)/2\varepsilon}$$

$$= \frac{\varepsilon}{W}$$

$$C = \frac{\varepsilon}{W} = \{\frac{\varepsilon q}{2}\,(\frac{N_a\,N_d}{N_a + N_d})\,\frac{1}{(V_{bi} \pm V_a)}\}^{1/2} \qquad (4.13.)$$

$$C \propto (V_{bi} \pm V_a)^{-1/2}. \qquad (4.14.)$$

Thus, the capacitance depends on the applied voltage, dielectric constant, area and the doping level. A plot of $1/C^2$ versus applied voltage is linear and extrapolates to V_{bi}.

For a linearly graded junction,

$$Q = \frac{q\,g\,W^2}{8} \qquad (4.15.)$$

$$V = \frac{q\,g\,W^3}{12\,\varepsilon} \qquad (4.16.)$$

and

$$C = \frac{dQ}{dV} = \frac{\frac{\partial}{\partial W}(q\,g\,W^2/8)dW}{\frac{\partial}{\partial W}(q\,g\,W^3/12\varepsilon)dW} = \frac{\varepsilon}{W}$$

or

$$C = \{\frac{q\,g\,\varepsilon}{12\,(V_{bi} - \frac{2kT}{q} \pm V_a)}\}^{1/3} \qquad (4.17.)$$

therefore,

$$C \propto (V_{bi} - \frac{2\,k\,T}{q} \pm V_a)^{-1/3}. \qquad (4.18.)$$

A plot of $1/C^3$ versus applied voltage is linear and extrapolates to $(V_{bi} - \frac{2kT}{q})$.

Heterojunction A junction between two dissimilar materials is called a heterojunction in contrast to a homojunction. Anderson (1962) treated the heterojunction by generalizing the result for the homojunction and obtained the depletion width and transition capacitance as the following:

$$W = \{\frac{2\varepsilon_1\varepsilon_2(V_{bi} - V_a)\ (N_{a2} + n_{d1})^2}{(q\ N_{d1} + N_{a2})\ N_{d1}\ N_{a2}}\}^{1/2} \qquad (4.19.)$$

where N_{d1} is the donor impurity concentration for first material and N_{a2} is the acceptor impurity concentration for the second material. The subscript "1" stands for material 1, "2" for material 2, etc.
Thus, the transition capacitance is given by

$$C = \{\frac{q\ N_{d1}\ N_{a2}\ \varepsilon_1\ \varepsilon_2}{2\ (\varepsilon_1 N_{d1} + \varepsilon_2 N_{a2})}\ \frac{1}{(V_{bi} - V_a)}\}^{1/2} . \qquad (4.20)$$

It is noted that, except for the slope changes, the plot of $1 / C^2$ will intercept at V_{bi} as was in the case of homojunction.

4.2 Current-Voltage Characteristics of P-N Junctions

4.2.1. Introduction

Under thermal equilibrium and in the absence of applied voltage, electron-hole pairs are generated within the semiconductor and are anihilated through recombination. This process is going on continuously. Since generation and recombination are balanced, no net current flows.

A p-n junction is an asymetric structure and an external voltage can be applied in two different ways. The polarity which makes the

p-region negative and causes the enhancement of the barrier height is called the reverse bias.

With the forward bias, the electric field across the space charge region is reduced resulting in the reduction of drift current. The balance between drift and diffusion currents is upset giving rise to a net current flow. Under reverse bias, on the other hand, the balance is upset in favor of the drift current. Thus, the primary effect of an applied voltage is to change the barrier height of the built-in potential which results in the flow of current since the drift and diffusion currents in the transition region are no longer balanced.

The above discussion is an over simplification of the real picture. The mechanism of current conduction is much more complicated and the mathematics so involved that simplification is needed to treat the problem adequately.

4.2.2. The Ideal Current-Voltage Equation

The first quantitative treatment of the current-voltage characteristics of a semiconductor diode was given by Shockley (1949) using the simplified model.

The assumptions made in deriving the so called ideal current-voltage equation are summarized as:

(1) Assume three distinct regions in the semiconductor: the neutral p-region, space-charge region and neutral n-region. The transition from one region to the other is also assumed to be abrupt.

(2) The semiconductor is not degenerate so that classical Boltzmann approximation can be applied. It can be shown that for most

of the semiconductors with reasonably wide band gaps, this requirement can be met easily.

(3) Assume low injection so that the disturbance from equilibrium is not large enough for non-linearity to set in.

(4) No generation in the space-charge layer.

(5) Geometrically a one dimensional model.

(6) Assume the band structure is homojunction (later will modify the case to heterojunction).

With all the assumptions, the current-voltage equation so derived is called the ideal equation since deviations are in the direction of poorer rectification. For instance, the violation of low injection will give rise to the case of high injection, the violation of no generation in the space charge region will result in the generation-recombination current and will be treated in modifying the ideal case. In other words, by assuming low injection or small currents, we are able to start with an equilibrium condition and arrive at a current-voltage relationship for a small disturbance. In equilibrium, two important facts obtain. These are (1) diffusion of holes and electrons in either direction and (2) drift in the presence of a field of holes and electrons in the opposite direction. The relationship between carrier density and voltage is found simply by requiring that the drift and diffusion currents be perfectly in balance.

At thermal equilibrium, the product of electron and hole densities throughout the semiconductor is constant. Thus,

$$p\, n = n_i^2 \qquad (4.21.)$$

When the bias is applied, the minority carrier densities on both sides of a junction are changed by a Boltzmann factor,

$$p\ n = n_i^2 \exp\left(\frac{q\ V}{k\ T}\right) \qquad (4.22.)$$

where p denotes the hole densities, n the electron densities, n_i the intrinsic density, q the electronic charge, V the applied voltage, k the Boltzmann constant, and T the absolute temperature in Kelvin. Based on the assumptions aforementioned, it was shown (see appendix 9.2.) that the ideal current-voltage equation can be given by

$$I = I_s \{\exp\left(\frac{q\ V}{k\ T}\right) - 1\} \qquad (4.23.)$$

where I_s stands for

$$I_s = q\ a\ \{\left(\frac{\bar{p}_{no}}{\tau_p}\right) L_p + \left(\frac{\bar{n}_{po}}{\tau_n}\right) L_n\} \qquad (4.24.)$$

L_p and L_n denote the diffusion length of holes and electrons, τ_p and τ_n the lifetime of holes and electrons, $\bar{p}_{no}$ the hole concentration in equilibrium at the depletion edge of the n-type semiconductor, $\bar{n}_{po}$ the electron concentration in equilibrium at the depletion edge of p-type semiconductor.

4.2.3. Deviations from the Ideal Equation

The ideal current-voltage equation of a p-n junction using the diffusion model as derived by Shockley (1949) gives a very simple result. This was the first time that the current-voltage equation was quantitatively derived based on the properties of the semiconductor. Experimental evidence has confirmed this theory for germanium diodes at low current densities. However, not all experimental results are in

such good agreement. With silicon no agreement was found.

The evidence of deviations are as follows: With reverse bias, no saturation was found with increasing voltage. In the forward direction, the characteristic curve does not show the theoretical shape. One way to observe the deviations is by comparing the slope of the characteristic curve plotted on a semi-log graph. The ideal equation predicts q V / k T slope while, in general, the practical diode shows a smaller slope.

The deviations are due to the violations of the assumptions made in deriving the ideal equation. They are: surface effects, generation and recombination of carriers in the depletion layer, and excess of minority carrier concentrations in the neutral regions. Heterojunctions with their discontinuous band structure at the boundaries also result in deviations.

Surface effects will receive separate treatment in the next section. Due to it's generalities, modification for heterojunctions will be reviewed separately. For purposes of analysis, it is convenient to divide the current-voltage characteristic into four regions after the treatment of Moll (1958).

(1) High reverse bias: According to the simple model of Shockley (1949), the reverse current is independent of the applied voltage. However, one observes an apparent departure from this by noting a breakdown at high reverse bias voltage.

The mechanism of breakdown was first identified to follow the theory of Zener. McKay et al. (1953) later showed that Zener breakdown only occurs in the thin depletion layers of p-n junctions with

highly doped materials. In lightly doped p-n junctions, having thicker depletion layers, the breakdown occurs as a consequence of charge carrier multiplication in the depletion layer and is known as avalanche breakdown.

Zener breakdown is explainable as a quantum mechanical tunneling effect. The reverse bias causes some overlapping of occupied and unoccupied bands. For tunneling currents, overlapping is not sufficient. The forbidden energy gap must also be sufficiently narrow in the horizontal direction. In other words, a minimal field must exist in the depletion layer of the p-n junction. The tunneling current has been described by

$$I_t = \frac{(2m^*)^{1/2} q^3 EVa}{4\pi^2 \hbar^2 E_g^{1/2}} \exp\left(-\frac{4(m^*)^{1/2} E_g^{3/2}}{3 qE \hbar}\right) \qquad (4.25.)$$

where E denotes the electric field, E_g the energy band gap, V the applied voltage, m^* the effective mass, a the area, and $\hbar = h/2\pi = 1.054 \times 10^{-34}$ Joule-sec.

For Si and Ge, a breakdown voltage of less than $4E_g / q$ is believed to be due to Zener breakdown. Breakdown voltage in excess of $6E_g / q$ is caused by avalanche multiplication. Between these ranges, a mixture of both mechanisms is observed.

Avalanche multiplication is by far the most important mechanism in breakdown. The close relationship between ionization by collision in p-n junctions and in gas discharges leads to the application of Townsend's theory for gas discharges in a somewhat modified form for p-n junctions.

Avalanche multiplication has been reported to possess properties which are distinguishable from Zener breakdown. In addition to the higher breakdown voltage, avalanche multiplication has a positive temperature coefficient of reverse voltage change in the breakdown region at constant current. Also, noise is significantly higher in the case of avalanche multiplication than for Zener breakdown.

The avalanche multiplication process may be described with reference to Figure 4.3. The minority carriers generated thermally in the neutral region adjacent to the depletion layer within one diffusion length may diffuse into the depletion layer. We assume the p-n junction to be reverse biased. Now, this stray "primary" carrier entering the depletion layer will be accelerated by the electric field to acquire a high kinetic energy which may be sufficient to cause the excitation of hole-electron pairs by an inelastic collision. The primary and the generated secondary carriers travel independently in the electric field and may cause further collisions, the total number depending on the ionization probabilities during each traversal of the depletion region by an electron or hole.

Although the avalanche process closely resembles the analogous phenomena in gases, the important difference consists in the fact that the path available for ionization in a p-n junction is restricted to the width of the depletion region.

The avalanche multiplication factor is defined as the ratio of the number of electrons leaving the depletion region (n) to the number of electrons entering the region (n_o) or

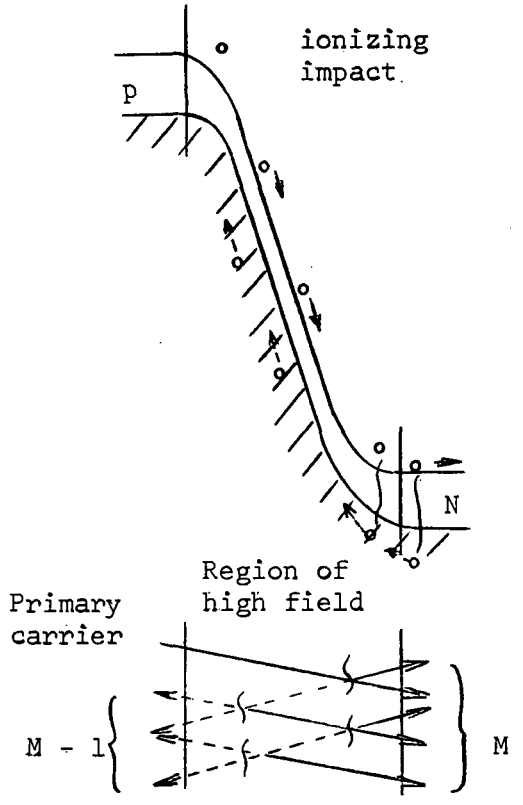


Figure 4.3. Avalanche multiplication caused by a "primary" electron

$$M = n / n_o \qquad (4.26.)$$

and can be expressed as (see Appendix 9.3.)

$$M = \frac{1}{1 - \int_{x_p}^{x_n} a_i\,(E)\,dx} \qquad (4.27.)$$

where $a_i(E)$ is the ionization rate, x_n the depletion length in n type semiconductor and x_p the same in p type semiconductor. Since the ionization depends on the field, the integral in equation (4.27.) for a given reverse voltage will also depend on whether the junction is an abrupt junction or a linearly graded junction. The multiplication factor M becomes infinite if

$$\int_{x_p}^{x_n} a_i\,(E)\,dx = 1$$

which means that the p-n junction breaks down.

For alloyed step junctions, Miller (1955) indicates that the multiplication factor can be found by the empirical relation

$$M = \frac{1}{1 - (V / V_b)^n} \qquad (4.28.)$$

where the exponent n has a value between 3 and 7 and the breakdown voltage V_b depends on the ohmic part of the p-n junction with high resistivity.

(2) Low and medium reverse bias: The departure from the "ideal" I-V characteristic for low and medium reverse bias is associated with the generation and recombination of carriers. Sah et al. (1957)

extended the ideal equation by including the effect of generation and recombination in the depletion region.

The generation and recombination rate involving a trapping center in the forbidden gap was given by Shockley (1952) to be

$$R = \frac{p\,n - n_i^2}{\tau_1 n_i + \tau_2 n + \tau_3 p} \qquad (4.29.)$$

Where τ_1, τ_2 and τ_3 are decay times, n_i is the intrinsic carrier concentration. Now, in the depletion region, we have $n < n_i$, $p < n_i$ and thus equation (4.29.) can be written as

$$R = -\frac{n_i}{\tau_1} \qquad (4.30.)$$

where τ_1 is the effective lifetime of minority carriers.

The current due to generation in the depletion region is given by

$$I_g = \int_0^W q\,a\,R\,dx \simeq q\,a\,|R|\,W = \frac{a\,q\,n_i\,W}{\tau_1} \propto n_i. \qquad (4.31.)$$

The current due to diffusion in the neutral region assuming $\bar{p}_{n0} >> \bar{n}_{p0}$ (i.e. one side is much heavily doped than the other) is from equation (4.24.)

$$I_s = q\,a\,\{(\frac{\bar{p}_{n0}}{\tau_p})L_p + (\frac{\bar{n}_{p0}}{\tau_n})L_n\}$$

$$\simeq q\,a\,(\frac{\bar{p}_{n0}}{\tau_p})\,L_p$$

$$= q\,a\,(\frac{D_p}{\tau_p})^{1/2}\,p_{n0}$$

$$= q\,a\,(\frac{D_p}{\tau_p})^{1/2}\,\frac{n_i^2}{N_d} \propto n_i^2 \qquad (4.32.)$$

where D_p is the diffusion constant in p type semiconductor in cm^2/sec.

The total current is approximately given by the sum of the diffusion components in the neutral region and the generation current in the depletion region. Therefore,

$$I = I_s + I_g$$

$$= q\,a\,\{(\frac{D_p}{\tau_p})^{1/2}\,(\frac{n_i^2}{n_d}) + \frac{W}{\tau_1}\,n_i\}$$

$$= A\,n_i + B\,n_i^2. \qquad (4.33.)$$

Where A and B are arbitrary constants, I_s the diffusion current in the neutral region, and I_g the generation current in the depletion region.

It is apparent from the above expression that I_g will dominate when n_i is small. A deviation from the classical theory of p-n junction occurs sooner if the intrinsic concentration n_i of the semiconductor material is smaller. The effects of generation may be expected for germanium ($n_i = 2.4 \times 10^{13}$ at room temp.) at relatively low temperature and for silicon ($n_i = 1.45 \times 10^{10}$ at room temp.) and for gallium arsenide ($n_i = 9 \times 10^{6}$ at room temp.) at any temperature. The comparison of the deviation is shown in Figure 4.4.

Generation current was shown to be proportional to depletion width W, which in turn is dependent on applied voltage. Therefore, we expect reverse current in the low and medium range to follow the power laws.

$$I_g \sim (V_{bi} + V_a)^{1/2} \qquad \text{for abrupt junction}$$

and

$$I_g \sim (V_{bi} + V_a - \frac{2kT}{q})^{1/3} \quad \text{for linearly graded junction.} \tag{4.34.}$$

(3) Low forward bias: If the generation current in the depletion layer is dominant for small reverse bias, this effect will also be dominant for low forward bias. As a result, more current will flow at low forward bias than is predicted by equation (4.23.). This explains the departure for silicon p-n junctions (and also GaAs) even at low biases.

(4) High forward bias: In the derivation of the ideal current equation, the assumption was made that no electric field exists in the neutral region. The current is then determined by minority carrier diffusion whereas the majority carrier current that maintains charge neutrality has the characteristic of a field current.

As the forward bias is increased, the effect known as high injection takes place. At high injection, the minority and the majority carrier concentrations may be of equal order of magnitude and equation (4.23.) has to be modified. Equations (4.21.) and (4.22.) can be combined to establish the inequality throughout the whole region

$$p\, n \leq n_i^2 \exp\left(\frac{q\, V}{k\, T}\right) \tag{4.35.}$$

where V includes the voltage (V_{bi}) associated with the field resulting from space charge as well as the applied voltage (Va).

The near equality of majority and minority carriers under high injection gives $p \simeq n$ and we have

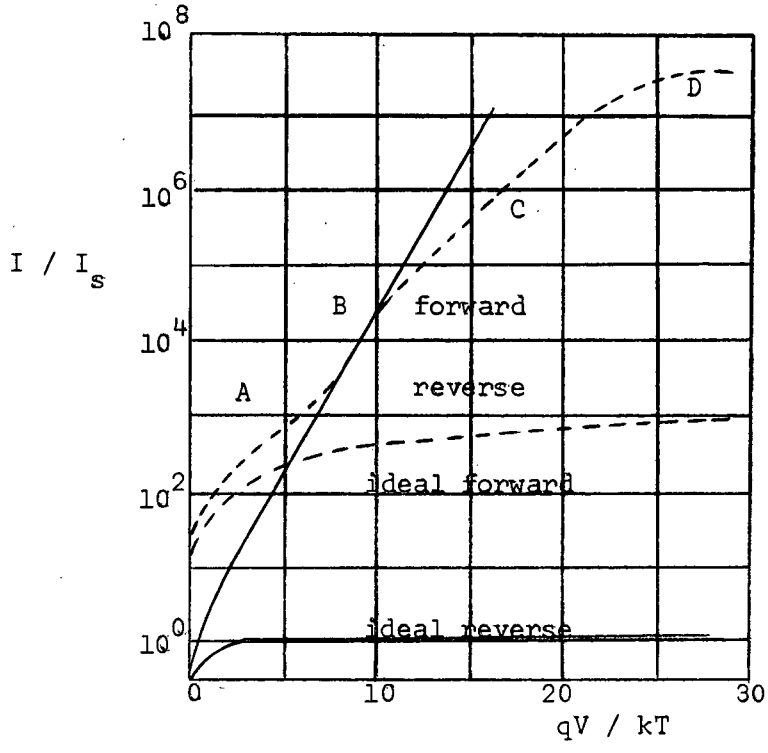


Figure 4.4. Comparison of an ideal and a real characteristic of a p-n junction including recombination in the depletion layer. Range A: recombination in the depletion layer is dominant. Range B: increasing influence of the diffusion current and approximation to an ideal one. Range C: high injection current. Range D: ohmic effect

$$p^2 \simeq n_i^2 \exp\left(\frac{qV}{kT}\right) \qquad (4.36.)$$

or

$$p \simeq n_i \exp\left(\frac{qV}{2kT}\right).$$

Thus, the rate of increase of minority carriers at high injection is slower than that at medium range where the current-voltage characteristic tends toward ideal behavior, and is in the direction of less current than predicted by equation (4.23.).

As the forward bias is further increased, the resistivity of the neutral region is no longer negligible and an ohmic effect is observed.

4.2.4. Modification Due To Heterojunction

A heterojunction is formed between two separate pieces of semiconductor with different band gaps. In addition to having different energy band gaps (E_g), the two semiconductors may have different dielectric constants (ε), different work functions (ϕ) and different electron affinities (θ).

Anderson (1962) proposed the energy band model of an ideal heterojunction neglecting generation-recombination current. The following description is given with reference to Figure 4.5. In part (a), since charge neutrality exists everywhere, the band-edge is flat. In part (b), a p narrow band gap and an n wide band gap are shown forming a junction. Several principles apply to Figure 4.5. The Fermi levels (E_f) again aligns throughout. The difference in the work functions (ϕ) between two materials is equal to the total built-in potential which will be distributed according to the ratio

$$\frac{V_{b1} - V_1}{V_{b2} - V_2} = \frac{N_{d2}\,\varepsilon_2}{N_{a1}\,\varepsilon_1}$$

where V_{b1} is the built-in potential supported by material 1, V_{b2} is same by material 2, and V_1 is the applied voltage distributed to material 1 and V_2 is same to material 2. In general, the work function for the wide band gap is smaller, therefore, the band edges will be bent as shown to account for the space charge. The electrostatic potential difference between two points is represented by the vertical displacement, and the electrostatic field is represented by the slope of the band edges. Because of the difference in dielectric constants in the two materials, the electrostatic field is discontinuous at the interface.

I-V Characteristics For a homojunction, the theoretical current-voltage characteristics of a p-n junction is derived to be of the form

$$I = I_s \{\exp (\frac{qV}{kT}) - 1\}. \qquad (4.37.)$$

The value of I_s is reasonabally independent of voltage applied. The diode equation is often written in the form

$$I = I_s \{\exp (\frac{qV}{nkT}) - 1\} \qquad (4.38.)$$

where n is an empirical factor which accounts for the disagreement between simple theory and experiment. It is found experimentally that for heterojunctions the diode equation (4.38.) is still applicable by fitting the proper empirical factor n. The theoretical justification was made by Anderson (1962).

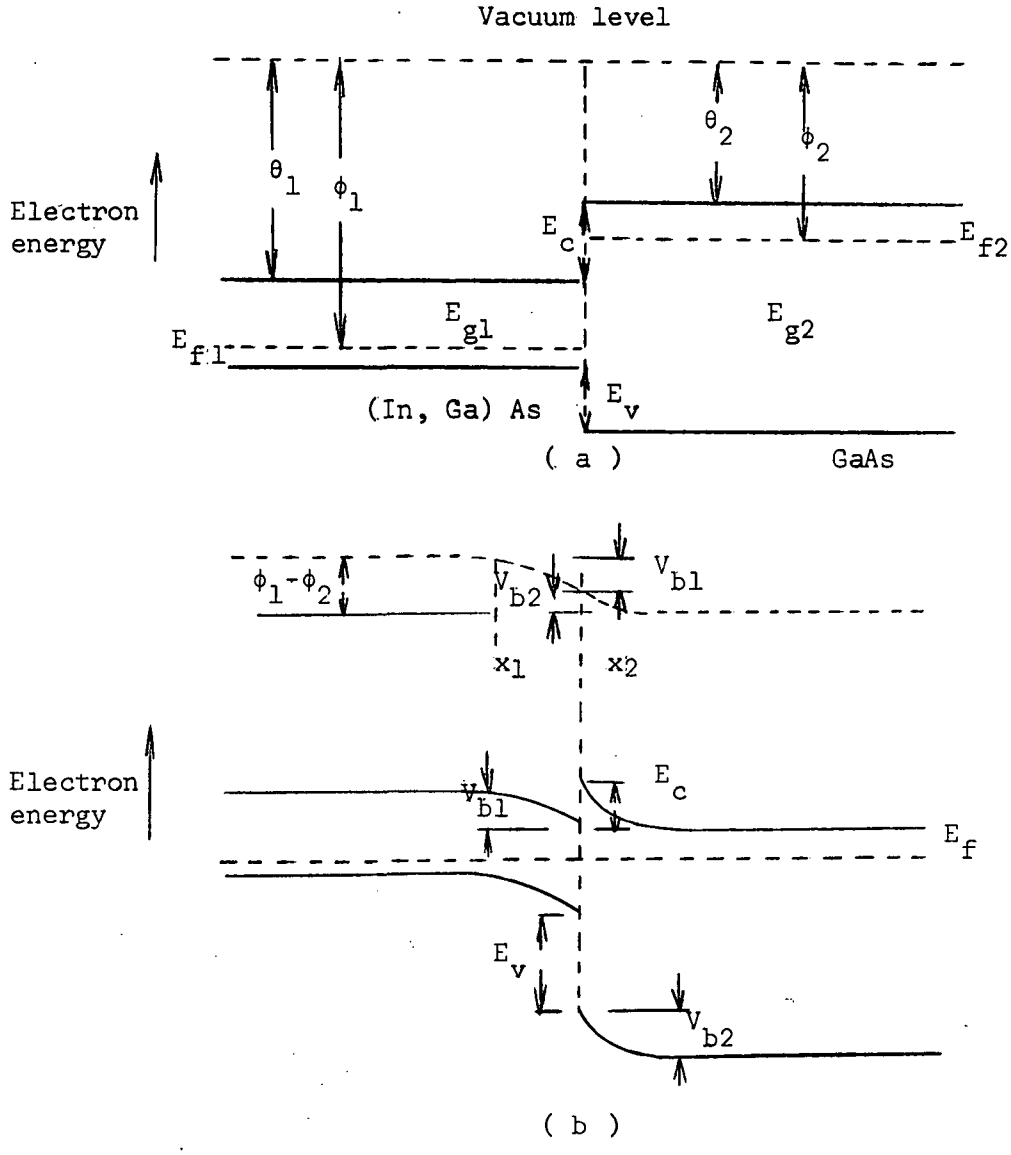


Figure 4.5. Energy band diagram of p-n heterojunction (a) before contact was made and (b) after contact was made

Theoretical justification: The discontinuities in the band edges at the interface represents a barrier to each of the two types of carrier flow across the interface and can result in essentially unipolar injection of carriers. This is quantitatively expressed as

$$I = M_1 \exp\left(-\frac{q V_{d2}}{k T}\right) - M_2 \exp\left(-\frac{q V_{d1}}{k T}\right) \qquad (4.39.)$$

where V_{d1} is the barrier that carriers in semiconductor 1 must overcome to reach semiconductor 2, and V_{d2} is the barrier to the carriers moving in the opposite direction. The coefficients M_1 and M_2 depend on doping levels, on carrier effective mass and on the mechanism of current flow.

Now, suppose in our model V_{d1} predominates so that the second term in equation (4.39.) is negligible compared with the first term, then on applying an external voltage, equation (4.39.) can be written as

$$I = M_1 \exp\left\{-\frac{q (V_{b2})}{k T}\right\} \left\{\exp\left(\frac{q V_2}{k T}\right) - \exp\left(-\frac{q V_1}{k T}\right)\right\} \qquad (4.40.)$$

where V_1 and V_2 are those portions of applied voltage appearing in materials 1 and 2 respectively. Equation (4.40.) consists of two terms, the first term in the brackets is important for forward bias and the second term for reverse bias. If $V_2 = V/n$ then $V = (1 - 1/n)V$ and the current varies approximately exponentially with voltage in both forward and reverse directions.

4.2.5 P-I-N Diodes

A p-i-n diode behaves qualitatively like an ordinary p-n junction

diode with a slightly higher forward resistance and a high reverse breakdown voltage.

Fletcher (1957) gives a simplified treatment of the p-i-n diode. The simplification consists in assuming that the diode is completely symmetric, and that the mobility as well as the diffusion coefficients for the holes and the electrons are exactly the same in each of the regions. The width of the i-region (2d) is assumed to be large compared with the width (g) of the p- and n-region. As a result, the electron concentration in p-region and hole concentration in n-region are assumed to vary linearly with distance as shown in Figure 4.6.

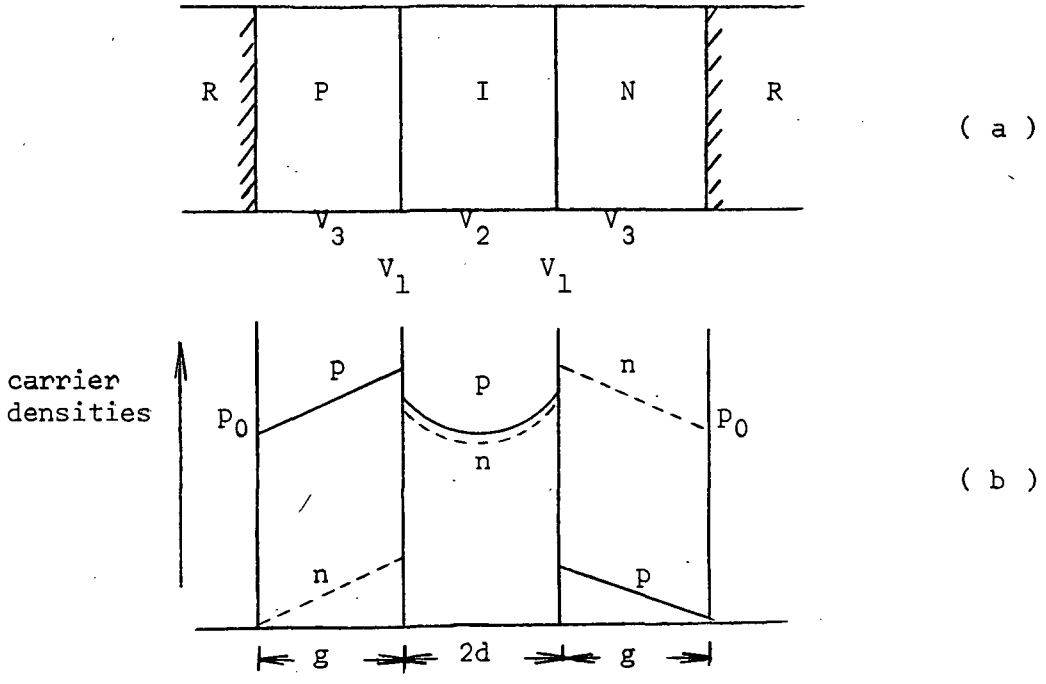


Figure 4.6. The p-i-n diode (a) junction profiles of the p-i-n diode; R are ohmic contacts (b) carrier density distribution in the diode (after Fletcher (1957))

With all the simplifying assumptions, Fletcher (1957) derived the diode current J to be

$$J = A \exp\left(\frac{e V_1}{k T}\right) + B \exp\left(\frac{2 e V_1}{k T}\right) \qquad (4.41.)$$

where we assume the total applied voltage to be

$$V = 2 V_1 + V_2 + 2 V_3 \simeq (2V_1 + V_2)$$

since $2 V_3 << 2 V_1 + V_2$. A and B are constants to be determined from the thickness of each region and from the bulk properties. Depending on the conditions, either the first or second term predominates.

With a very short i-region, the first term in Equation (4.41.) is negligible, and the I-V characteristic varies as exp ($2 e V_1/k T$) or as exp ($e V / K T$) since $V_2 << 2 V_1$ and $V \simeq 2V_1$. With a rather thick i-region, the first term predominates and the I-V characteristics vary as exp ($e V_1 / K T$), or as exp ($e V / 2kT$). In general, the I-V characteristics for p-i-n diode can be written in terms of the applied voltage as

$$I = C \exp (e V / m k T)$$

where $1 \leq m \leq 2$; $m = 1$ for very thin diodes and $m = 2$ for thick diodes.

4.3. Theory of Surface

4.3.1. Introduction

The bulk properties of crystals are well understood and are more defined than surface properties. The periodicity of the crystal leads to the elegant theory of a band structure, and consequently the concepts of crystal momentum and effective mass. At the surface, however, the periodicity suffers an abrupt termination and therefore the theory

developed in the bulk has to be modified accordingly.

The direct consequence of the termination of periodicity is that the interatomic valancy "dangle" (absence of covalent bonding) on the surface which tends to trap electrons or interact with adsorbed foreign atoms. A real surface is never clean. Surfaces are usually covered with an oxide layer or are contaminated with foreign species. Adsorbed chemical impurities produce mirror image charge inside the bulk. This results in an inversion layer, accumulation layer, or depleted layer immediately underneath the surface and greatly affects the conductivity of the surface layer.

Another significant consequence is that surface states will exist in the forbidden gap where electron energies are otherwise not allowed. This is because the energy band picture was developed by assuming a periodic and symmetrical electron potential function, and since this symmetry is upset at the surface, the usual distribution of allowed electron energy states is altered in the surface layer.

Trapping levels distributed in the band gap can act as recombination centers and affect the surface lifetime. One type of state responsible for surface recombination of electrons and holes is located at the interface of the semiconductor and semiconductor oxide film.

Another type of surface state is located at the surface of the oxide with perhaps some states in the oxide film. These states result mainly from adsorbed gas molecules. Depending on the ambient gas, they are either predominantly p-type or n-type. It is principally these states which determine the bending of the bands at the surface.

In terms of the time constant of the surface states, the former is orders of magnitude less than the latter, therefore they are called fast states. However, since slow states are ionic in nature, they are primarily responsible for the induced surface layer charge in the interior of semiconductor.

Our primary interest in the semiconductor surface is in the understanding of the properties of semiconductors controlled by the surface treatment and the ambient gases. In this section, some of the basic surface properties will be reviewed, and the methods of measurement will be briefly mentioned. Finally, the surface treatment and its effect on the reverse breakdown will be considered.

4.3.2. Surface Properties

The surface of a solid in general and a semiconductor solid in particular is always characterized by the abrupt termination of the periodicity of the crystal lattice resulting in localized states within the forbidden gap. The region is less than the mean free path of electrons. Therefore, for practical purposes, it can be thought of as a thin layer. However, the thin layer posseses a very particular property in that it may include trapping of electrons or holes, and, as a result, unneutralized electrical or ionic charges may be accumulated.

Surface Charge For simplicity, assume electrical charges exist on the semiconductor surface. Then, depending on the magnitude as well as the polarity of the attached charge and also on the conductivity type of the bulk semiconductor, different energy band structures will obtain as shown in Figure 4.7.

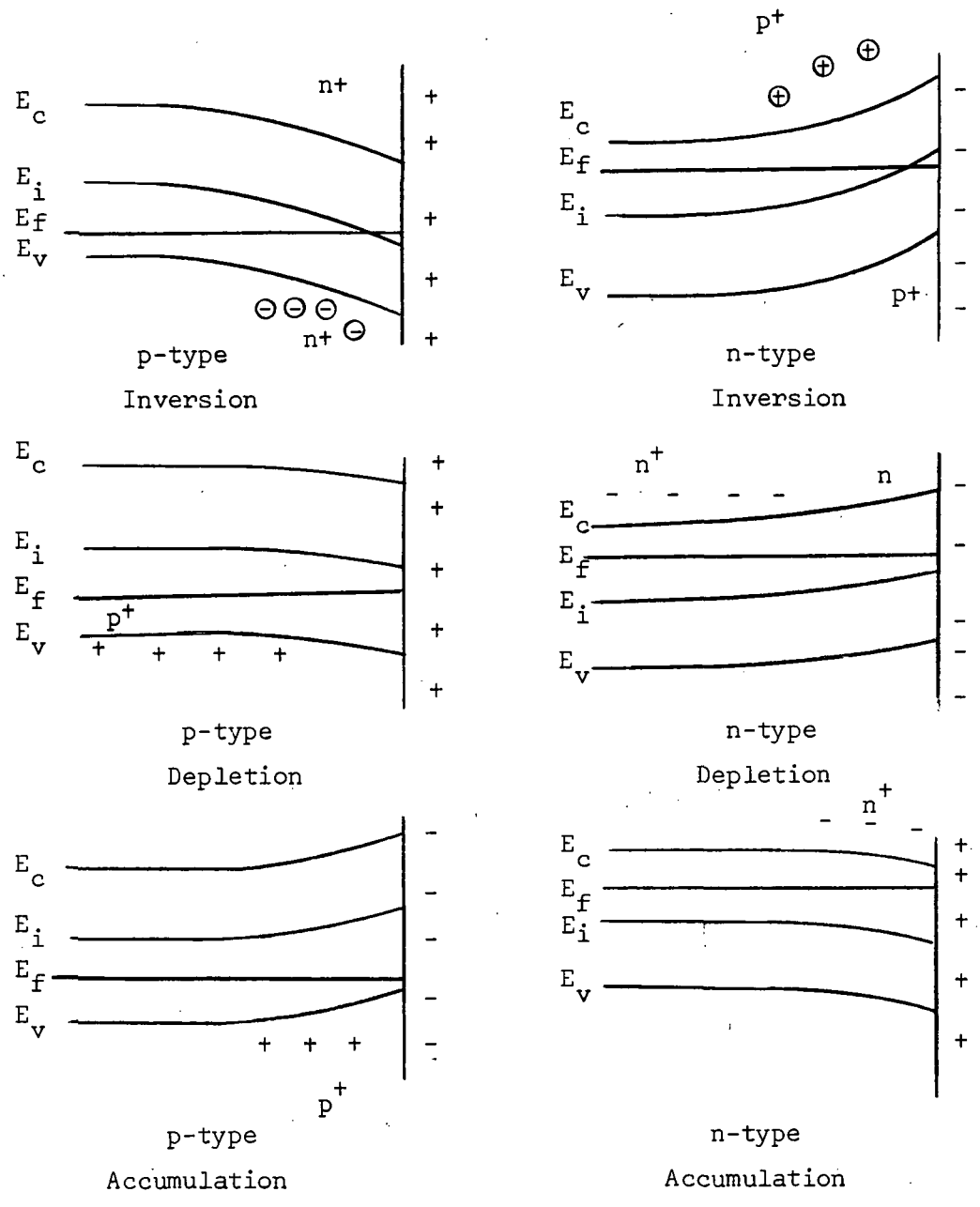


Figure 4.7. Energy band profile at the surface. All + and - signs represent the mobile holes and electrons. While ⊕ and ⊖ represent the space charge resulting from immobile donor atoms. n^+ denotes that the electron concentration is slightly higher than elsewhere in the semiconductor, while p^+ denotes the same for holes.

Only one characteristic is common: electrical charges of opposite sign reside in the interface. If the sign of the charges on the surface is opposite to that of the majority carrier in the bulk semiconductor, the charges on the surface will attract majority carriers to the surface, thereby forming an accumulation layer. If the sign of the charges on the surface is the same as the majority carrier in the bulk semiconductor, two cases may arise depending on the magnitude of the charge. If the magnitude is moderate, the surface layer is depleted of carriers. For a larger surface charge the surface layer may become inverted by attraction of minority carriers to the surface layer. Whatever the case, the surface layer charge is uncompensated, and we can solve Poisson's equation for the uncompensated charge to yield a finite electrostatic field. This field is mainly responsible for the bending of energy bands on the surface. Also, it is evident from the energy band diagram that in order to invert the conductivity type at the surface, the charge has to be large enough to bend the energy band so that E_i will cross E_f.

Trapping States on the Surface The surface states are localized states on the surface of semiconductors. These states act like traps which capture holes or electrons. Pictorially the traps may be described as a neutral impurity atom in a crystal lattice that has the ability to capture electrons or holes. If such an atom captures an electron, it is charged negatively and has the ability to attract a hole. The association of a hole with an electron corresponds to recombination. The capture time may be long or short depending on the location of the state. The results of measurements indicate that the

"fast" state resides at the interface between the semiconductor and the oxide layer and mainly involves the recombination processes. The "slow" state exists on the surface outside the oxide layer, and the charge is believed to be ionic in nature.

Ionic Surface Charge We may have two types of charges on the surface. One type is from electrons or holes which diffuse through the oxide and migrate to the surface. The other is the ionic charges which are adsorbed on the surface. Since the process involved in changing the ionic charge density is relatively slow, it is primarily the ionic charges which produces the surface layer charges. This explains why the holes and electrons in the interior of a semiconductor are so sensitive to changes in the ambient gases and surface treatment.

Contact Potential and Work Function The work function of a solid metal or a semiconductor is defined as the difference between the energy of a free electron outside the solid and the fermi level E_f. Figure 4.8. shows the work function for various cases. The contact potential is the difference $(\phi_1 - \phi_2)$ between the work functions ϕ_1 and ϕ_2 of two materials in contact. Contact potential is a very important parameter in exploring surface properties.

4.3.3. Measurement of Contact Potential

Surface conductance, recombination velocity, field effect and contact potential are some measurable quantities which have been successfully used to explain surface properties. Measurement of contact potential has some historical interest and is related to our work with surface treatments and ambient gases. Therefore, a brief description is

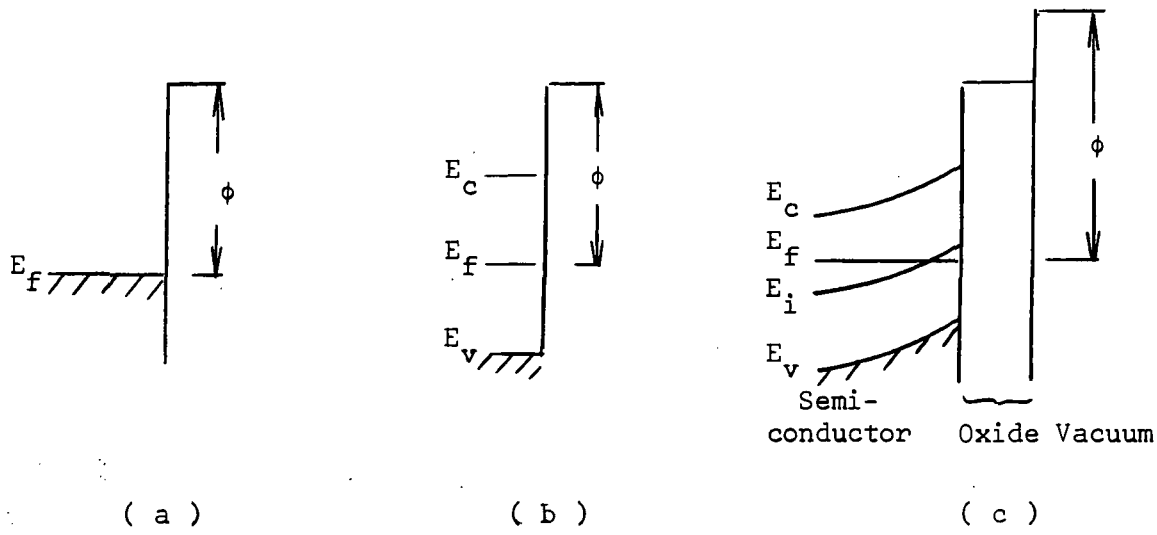


Figure 4.8. Schematic diagram showing work function for (a) metal, (b) semiconductor and (c) semiconductor-oxide layer

in order.

In the study of surface effects, one is tempted to measure work function of a semiconductor. However, experience tells us it is a fruitless effort to attempt to obtain detailed information from the direct measurement of work function.

A more sophisticated scheme is to use the Kelvin method in which a reference electrode vibrates near the semiconductor surface. The difference in electrostatic potential is detected as an ac signal at the vibration frequency. A dc bias between the semiconductor and the reference electrode is adjusted for a null in the ac signal. Thus, in principle, changes in work function are measured. However, in order to

produce a change, it is necessary to change the ambient gases. Such changes also affect the work function of the reference electrode. One way to avoid changing the environment is to illuminate the surface of the semiconductor and note the changes in contact potential.

Brattain et al. (1954) used a semiconductor-electrolyte system and measured the contact potential difference between a semiconductor and a reference electrode when both are submerged in the electrolyte.

4.3.4. Surface Treatment and Gaseous Ambient

In his study of germanium surface phenomena, Kingston (1956) catalogued the relative contact potential and ambient as shown in Table 4.1.

Table 4.1. Surface contact potential vs ambient

$H_2O + N_2$	n-type	ϕ_s negative
H_2O + air		
$H_2O + O_2$		
N_2 (dry)		
Air (dry)		
O_2 (dry)		
H_2O_2 (peroxide)		
O_3 (ozone)	p-type	ϕ_s positive

From the table it is shown that wet nitrogen produces the strongest positive surface change (n-type layer in semiconductor) and ozone yields the largest negative change (p-type layer in semiconductor). Dry air which is in the middle of the list and nearly neutral, is the preferred atmosphere in device fabrication.

Surface Treatment: The surface can be treated mechanically by bombarding the surface, and thus creating more surface states. Excess electrons or holes striking the surface are either trapped or recombine. The surfaces thus obtained are said to be p-type.

On the other hand, chemically treated surfaces are more involved and the mechanism of absorption or desorption are not wholly understood. However, disregarding the mechanism be it ionic affinity or chemical absorption, our primary interest is in the polarity as well as the magnitude of charges on the surface so that surface properties can be determined.

Brattain et al. (1954) regarded the surface as a discrete semiconducting phase and suggested that the properties may be changed by altering the chemical nature of the surface. For anodic bias, the important reaction is $X^- + p \rightleftarrows X$ and likewise for cathodic bias $Y^+ + n \rightleftarrows Y$.

If the surface treatment is by chemical etching or a chemical bath, the proper choice of etchant and chemical solution has to be made depending on the surface conditions (p-ness or n-ness) and surface affinity. At the present stage, the chemistry of surface treatments is not well understood, therefore no definite procedure can be followed. Guesswork plus trial-and-error has to precede the analysis.

In general, it is desirable that the surface treatment produce a low surface recombination velocity (rate at which carriers recombine) and consequently a low interface state density. Buck et al. (1958) in his study of silicon surface properties concluded that low recombination velocity occurred when the surface was strongly p-type or when it was strongly n-type.

However, the surface recombination velocity cannot be measured easily. If the device is a p-n junction, an alternate way to measure the "improvement" of the surface is by taking the current-voltage characteristic curves. The "ideality" of the forward characteristic can be taken as a measure of the surface condition.

The reverse current-voltage characteristic is also a very sensitive parameter of the surface condition. An improperly prepared surface can cause breakdown at low reverse bias voltages. An inversion layer near the junction provides a leakage channel in the device. Appropriate surface treatments can provide a trade-off between breakdown voltage and excess reverse leakage current.

5. EXPERIMENTAL RESULTS AND ANALYSIS

5.1. Capacitance-Voltage Characteristics and Its Interpretation

Capacitance versus reverse voltage measurements were made on all samples. The results were used to plot $1/c^2$ and $1/c^3$ versus applied voltage. A $1/c^3$ relationship appears to fit the data. Thus, from the theory derived in 4.1.2. we conclude that all the devices are linearly graded junctions.

Using the measured capacitance (take for example I-E-1) and approximating the junction capacitance as a parallel plate, we obtained a depletion width from d = 10 microns (corresponding to C = 320 pf) to d = 22.6 microns (corresponding to C = 150 pf). This estimate appears to be a typical range for all the fabricated devices in either group.

A detailed comparison cannot be made between group I and group II merely from the data obtained in C-V measurements. However, from the exterpolated intercept of C-V curves in Figure 5.2., I-E-1 sample gives here a zero capacitance intercept larger than the band gap of gallium arsenide which is indication of intrinsic layer formation. The extended intercept in I-E-1 is explainable as an extra voltage drop (greater than bandgap) across the intrinsic layer in Zn-(In, Ga)As junction. All the Zn-GaAs junctions in group II have a consistent intercept at 1.3 volts.

A rough estimate using LSS (Lindhard, Scharff and Schiott) range statistics of the projected range for the 60 Kev Zn ion beam into GaAs is approximately 0.0277 microns. The thickness of the semi-insulating layer formed during ion-implantation is reported by Hunsperger *et al*.

(1968) to be dependent only on the substrate background impurity concentration, and was estimated to be approximately 1.2 microns for GaAs of 5 x 10^{16} cm^{-3} concentration. The implanted junctions for each group are depicted in Figure 5.1.

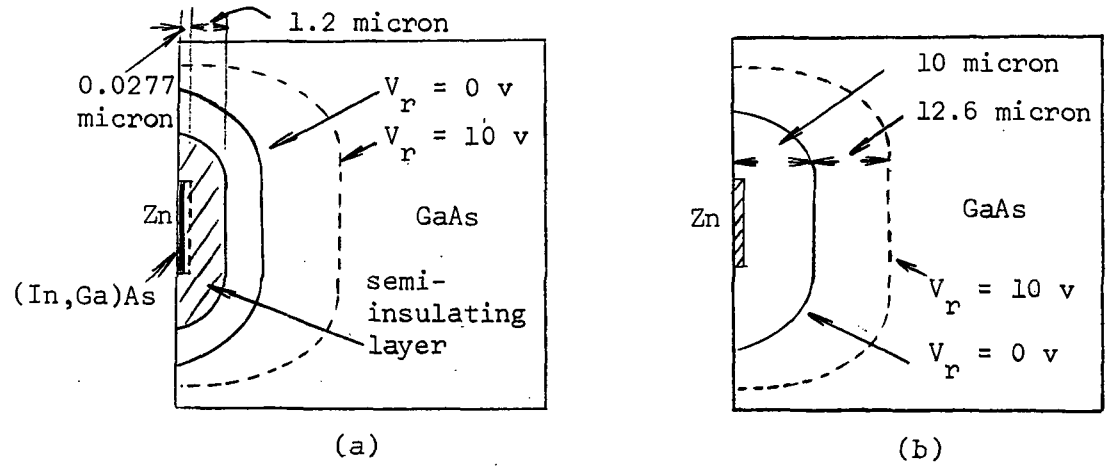


Figure 5.1. Sketch of junction profiles for (a) Zn-(In, Ga)As and (b) Zn-GaAs

Capacitance-voltage measurements show a slight decrease in capacitance as frequency is increased. This might be due to deep traps created by ion implantation as reported by Hunsperger et al. (1968). The decrease at higher frequencies is due to the charged carriers at deep trapping level that cannot change with the applied voltage, hence a partial loss in capacitance.

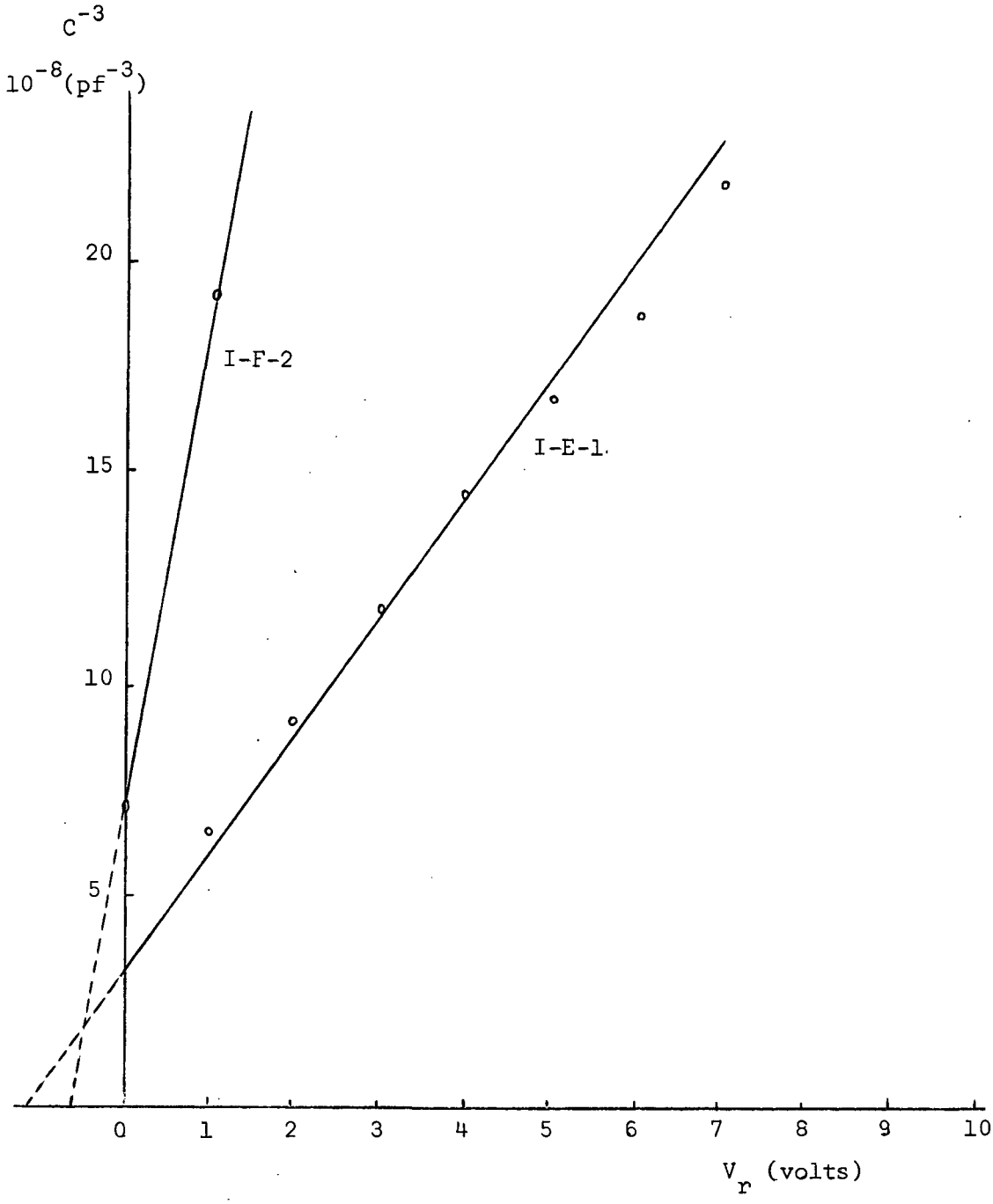


Figure 5.2. A plot of C^{-3} versus reverse voltage (group I)

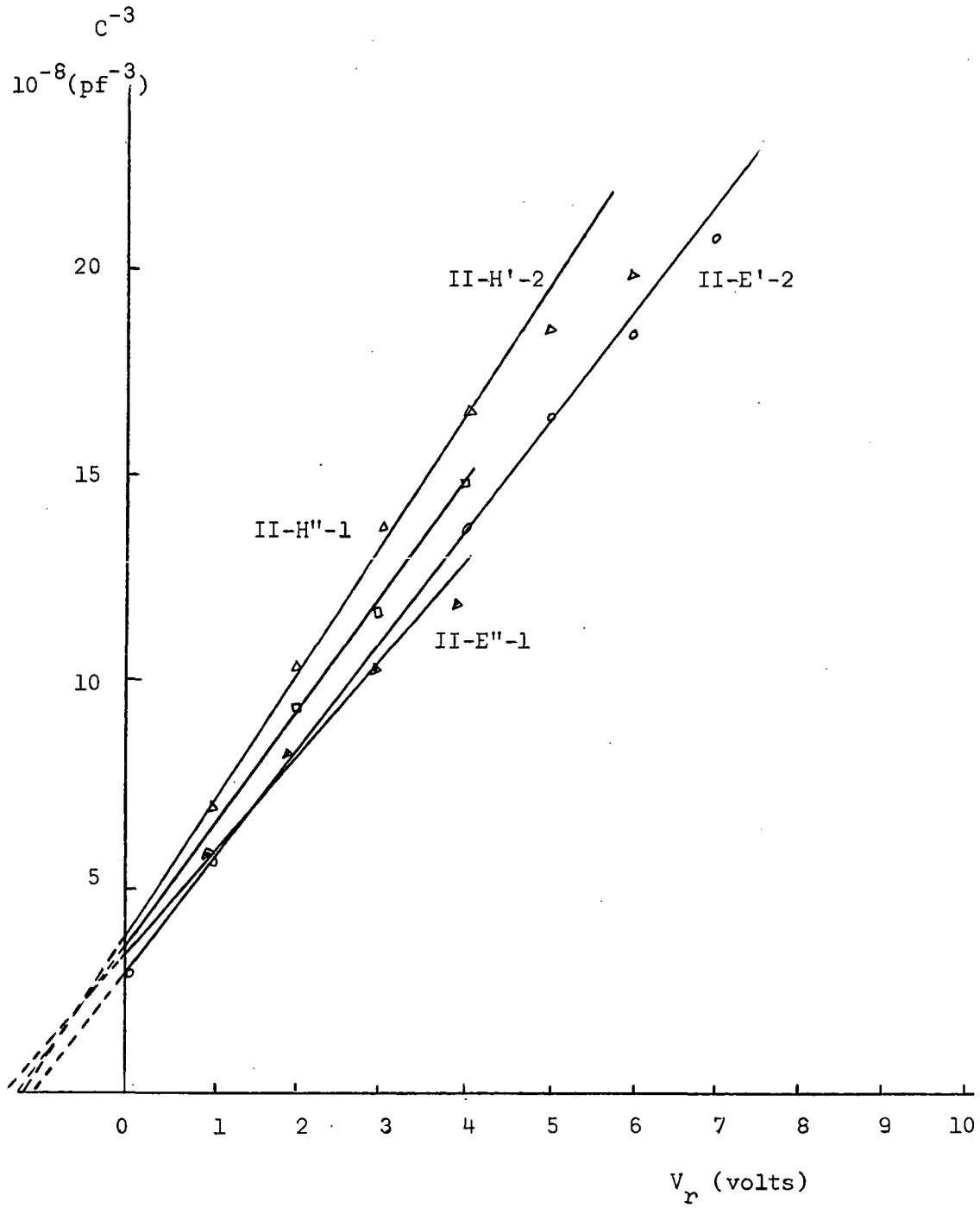


Figure 5.3. A plot of C^{-3} versus reverse voltage (group II)

5.2. Current-Voltage Characteristics and Its Interpretation

The current-voltage characteristics of each group have been plotted on the same graph paper so as to facilitate the comparison. The values of n were found empirically by fitting data to the expression

$$I = I_s \exp (qv/nkt).$$

Figure 5.5 shows forward I-V characteristics for group I which are Zn-(In, Ga)As junctions. Except for I-E-2, I-H-1 and I-H-2, the rest of the devices show consistent characteristics over three regions. From V_f = 0v to 0.2v is identified as the A region, from 0.2v to 0.6v as the B region, and 0.6v to 1.0v as the C region. Both region A and C are linear in I-V characteristics and are ohmic in nature. Region A is believed to be due to the surface leakage while region C is essentially an ohmic effect. For the purpose of analysis, the results are resolved into components consisting of linear terms and an exponential term (see Figure 5.4.). The latter takes care of the current through the junction while the former takes into account the surface leakage current as well as ohmic effects in the bulk at high currents. If the surface leakage current predominates in the small forward bias, it should also exist in equal proportion at moderate reverse bias. This is actually the case as can be seen after comparing Figure 5.7. with Figure 5.4. (Figure 5.4. is plotted on an expanded scale). Therefore, the forward I-V characteristics can be resolved into surface and bulk components. Thus, it can be written

$$\begin{aligned} I_f &= I_{SF} + I_d \\ &= C_1 V + C_2 \exp (qV/nkt) \end{aligned} \qquad (5.1.)$$

Where I_{SF} represents the surface leakage current and I_d the diode current through the bulk. In Figure 5.4. I_f has been resolved into components. It is evident from the same figure that the surface leakage current predominates in region A. Region B has a defined slope and has been empirically fitted to the exponential term yielding n = 1.1. Region B is believed to be diffusion dominated; with the surface leakage current small compared to the junction current. A small deviation from the ideal diode current as observed in region B is possibly due to a semi-insulating layer formed in or near the p-n junction. As a result, the externally applied voltage will be proportionately distributed over p-i and i-n junctions. The effect of the semi-insulating layer upon the I-V characteristics can be analyzed using the results in Section 4.2.5. In the derivation of p-i-n diode characteristics, two cases were considered: $d/L = 1$ and $d/L \ll 1$, where 2d denotes the thickness of the intrinsic layer and L the diffusion length of the minority carriers in this layer. At low current for both cases, the diode current is given by $I = B \exp(qV/kT)$. This is also a good approximation for the case of $d/L \ll 1$ at high current. It is only for the case $d/L \approx 1$ and at high current that deviation from the ideal characteristics becomes appreciable, i.e. for this case, the I-V characteristic is approximately given by $I = A \exp(qV/2kT)$. Between these two extremes, n takes on values between 1 and 2. For the sample in question, $I = C \exp(qV/1.1\ kT)$, which indicates that the intrinsic layer is not thick enough to cause any appreciable deviation from the ideal characteristics.

Region C is at a higher bias voltage, where ohmic effects should be considered. Since Indium was ion-implanted into GaAs, we expect heterojunction formation in the device. The optical data obtained from separate experiments indicates that an (In, Ga)As layer is formed. However, the evidence from I-V characteristic indicates that the mismatch in the heterojunction is not big enough to cause any appreciable effect on the I-V characteristics.

Except for different degree of surface leakage, the reverse I-V characteristics for Zn-(In, Ga)As devices are approximately the same. Reverse bias breakdown did not occur over the range of voltages used in the measurements. In contrast to the Zn-(Ga,As) devices which, due to generation-recombination current, follow a power law reverse characteristic, there was no indication that the Zn-(In,Ga)As devices are generation-recombination dominated. The existence of an intrinsic or semi-insulating layer in the Zn-(In,Ga)As devices could be responsible for the observed differences.

Figure 5.6. shows forward I-V characteristics for goup II devices which are Zn-GaAs p-n junctions. Except for the single device II-E"-2 this group shows consistent results. In contrast to the group I devices, they have less surface leakage as evidenced by the extended exponential region. Therefore, the characteristic curves have two regions - one is from 0.2v to 0.7v and the other is from 0.7v to 1.0v. Over the first region n is approximately unity which suggests a diffusion dominated current. The bending in the second region is thought to be an ohmic effect.

The reverse I-V characteristics for goup II devices can be approximated by the power law $I \sim V^{1/3}$, which indicates a generation-recombination dominated current. As has been explained in Section 4.2.3.-(2), generation-recombination current is proportional to depletion width W, which in turn is dependent on applied voltage. Unless the available charged carriers are exhausted an intrinsic region such as that suggested for the group I devices, the generation current Ig will contribute appreciably to the reverse current Ir, resulting in the power law reverse I-V characteristics.

Reverse bias breakdown was not observed in the range of measurement taken for the GaAs devices.

In summary the experimental results are: (1) The Zn-(In, Ga)As junctions of group I are characterized as p-i-n heterojunctions. (2) The thickness of the semi-intrinsic layer and the mismatch in heterojunction does not greatly influence the diode characteristics. (3) Due to a semi-intrinsic layer, generation-recombination currents were not observed. (4) Surface properties resulting from ion-implantation give rise to an appreciable surface leakage current. (5) The Zn-GaAs junctions of group II are characterized as p-n homojunctions. (6) In the absence of a semi-intrinsic layer, a generation-recombination current does exist in the group II junctions. (7) The I-V characteristics of group II junctions are simpler than group I junctions due in part to the absence of surface leakage current at low forward bias.

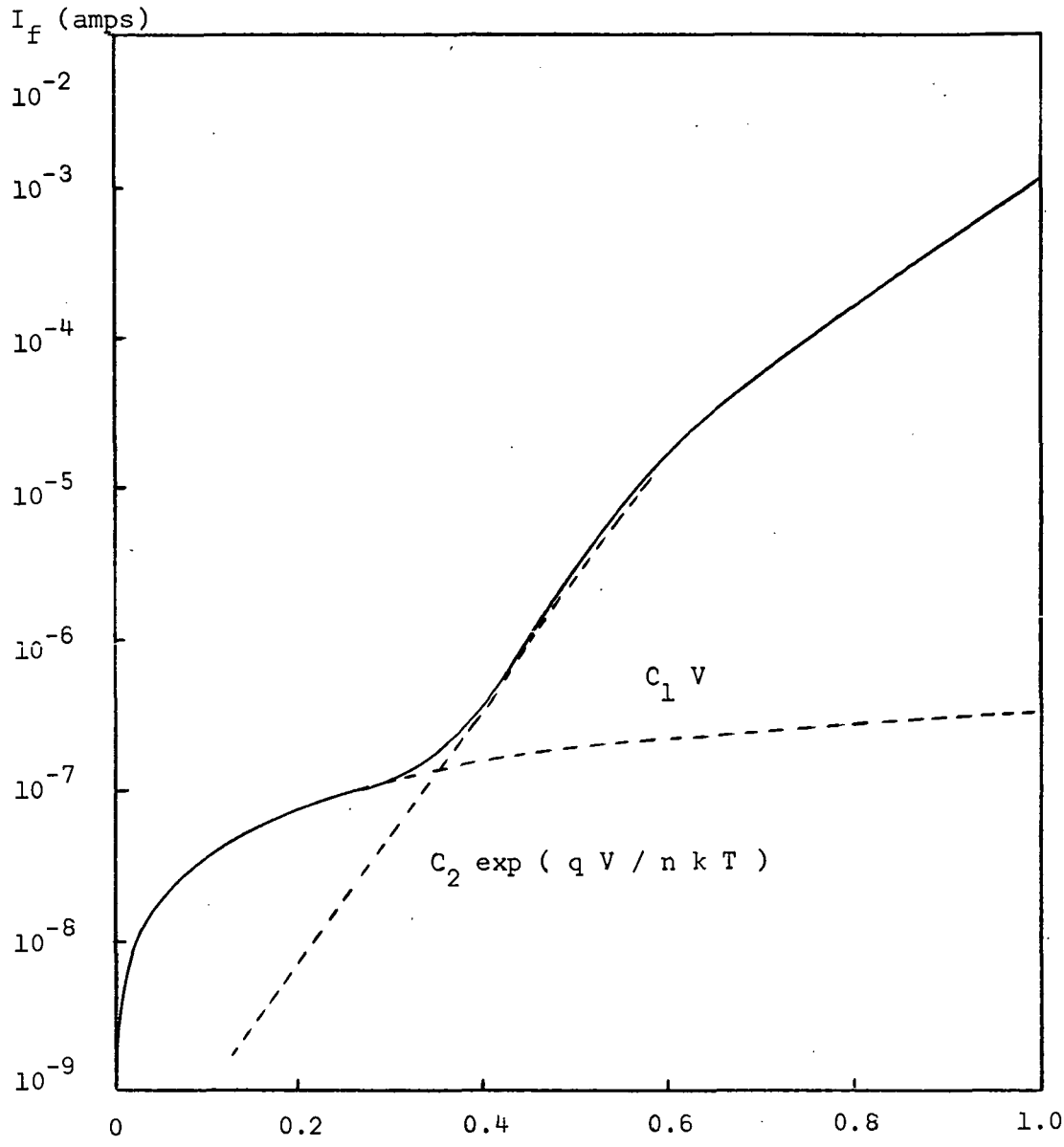


Figure 5.4. Forward I-V characteristic of I-E-1 illustrating that the current I_f can be resolved into components consisting of a linear term (the surface leakage current) and an exponential term (the diode current)

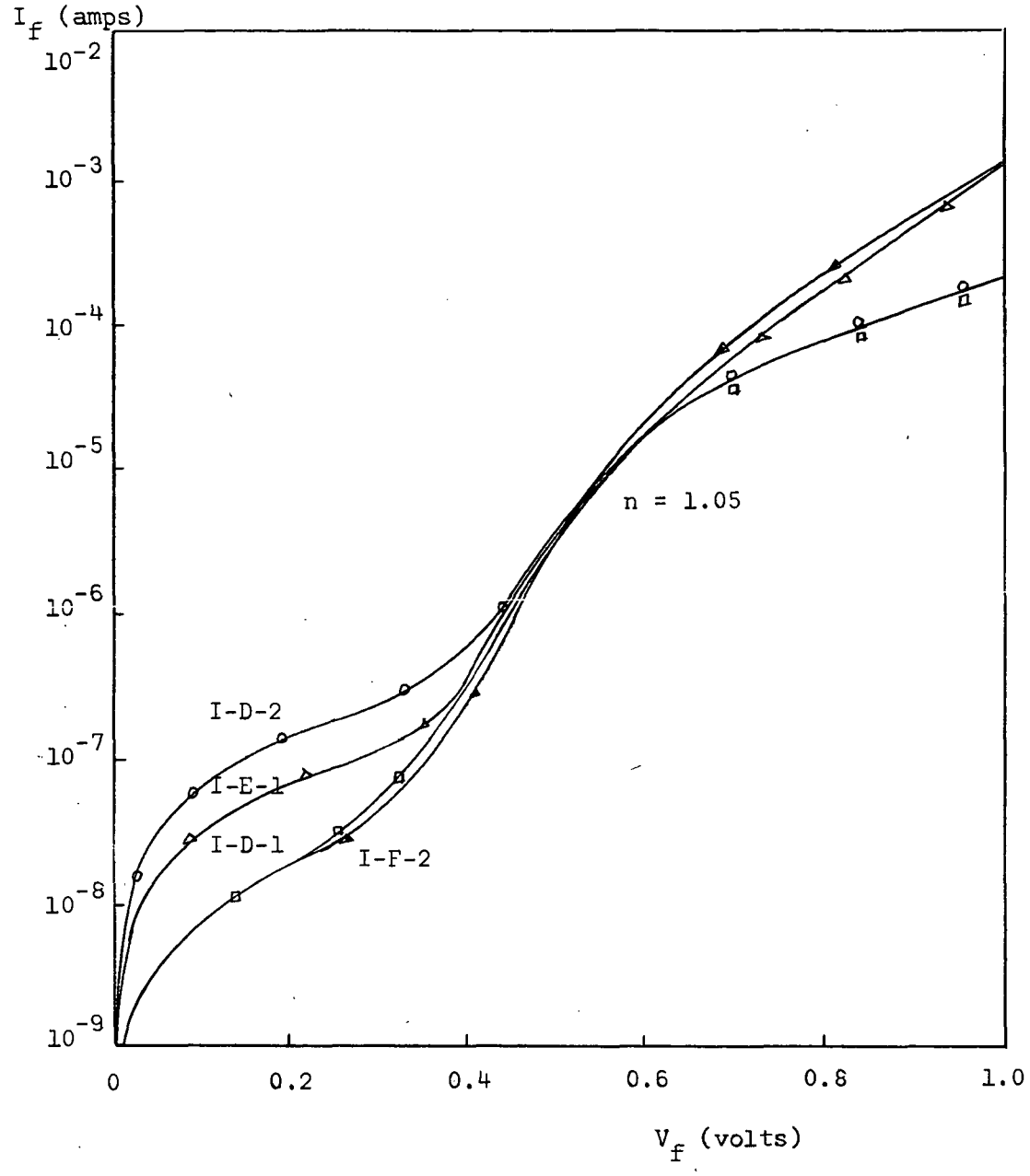


Figure 5.5. Forward I-V characteristics for Zn-(In, Ga)As junctions. The indicated values of n are found by empirically fitting the expression $I = I_s \exp (ev / nkT)$

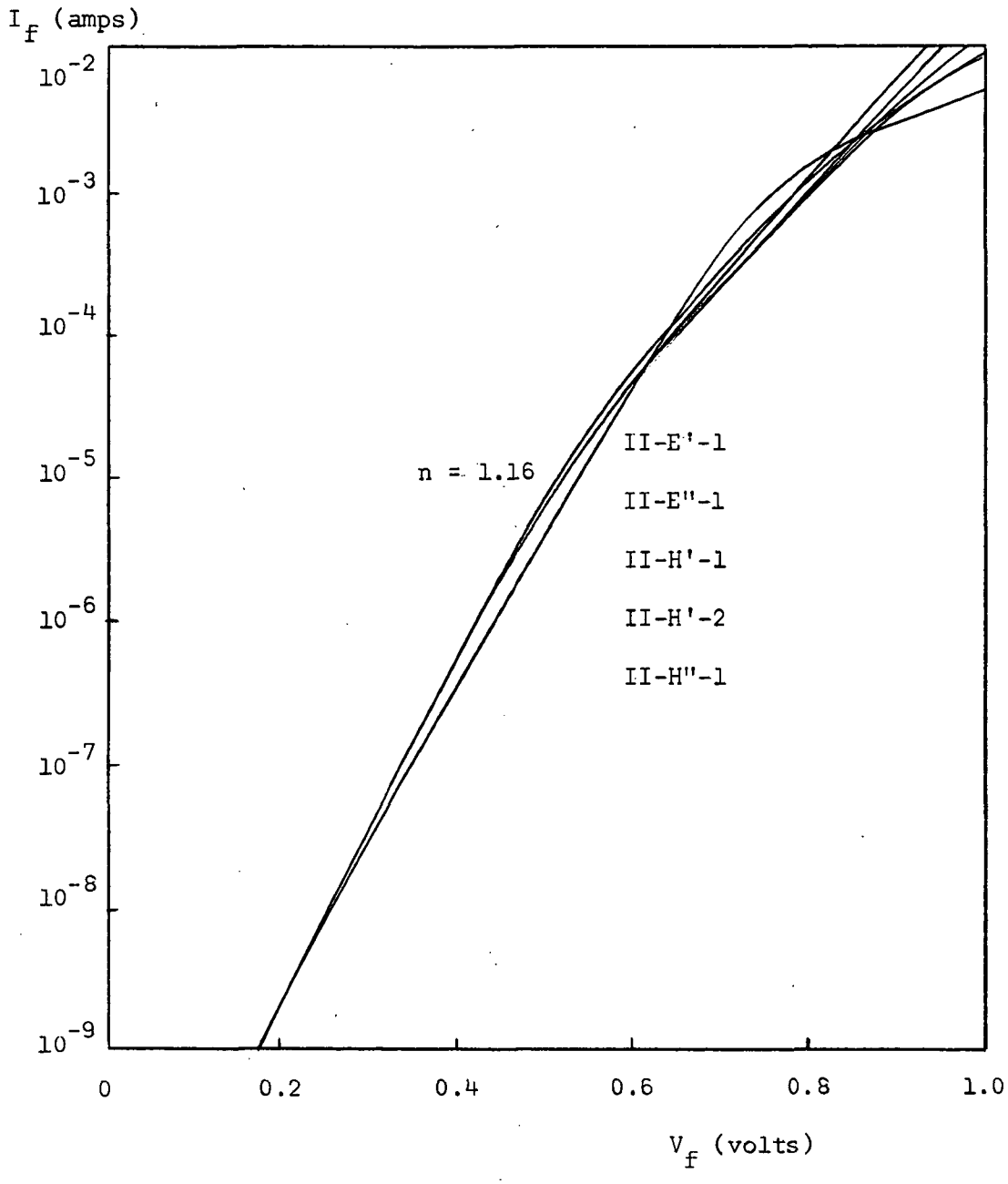


Figure 5.6. Forward I-V characteristics for Zn-GaAs junctions. The indicated value of n is found by empirically fitting the expression $I = I_s \exp (ev / nkT)$

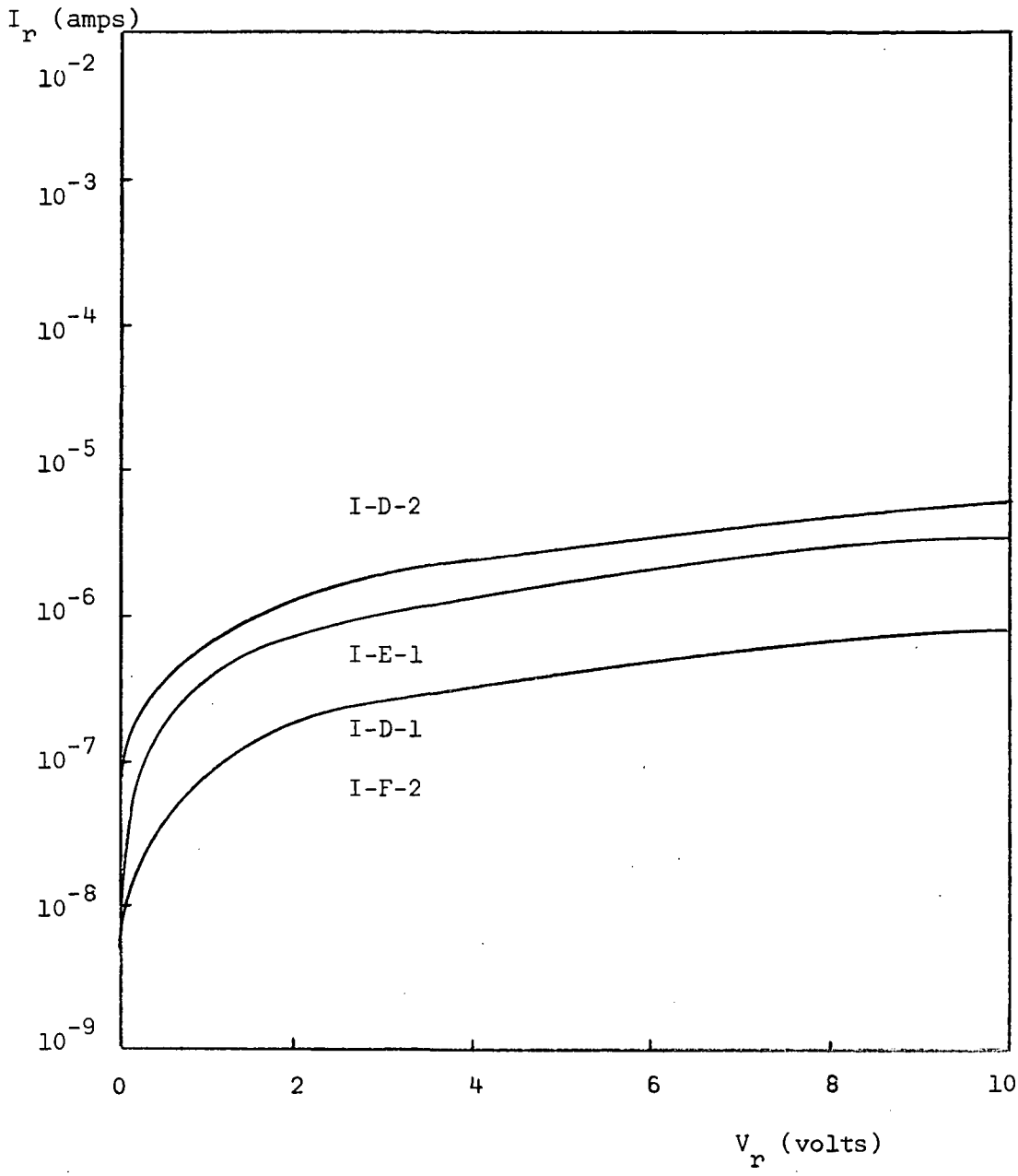


Figure 5.7. Reverse I-V characteristics for Zn-(In, Ga)As junctions

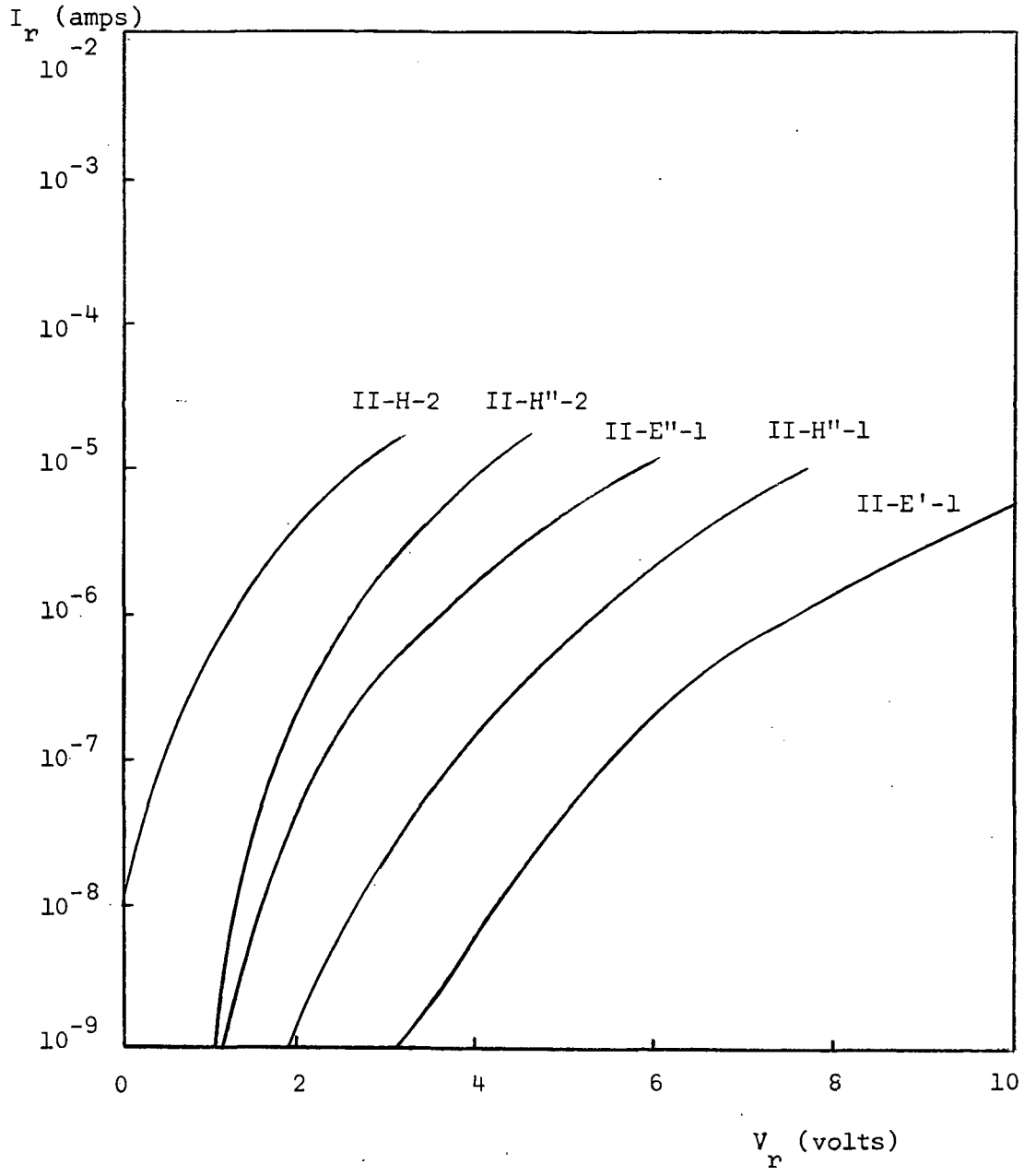


Figure 5.8. Reverse I-V characteristics for (Zn-GaAs) junctions

5.3. Surface Treatment and Reverse Breakdown Voltage

Surface treatments were carried out on two samples (I-E-1 and II-E'-1), one from each group.

Early in the research program, exposure to various ambient gases and chemical treatment of the surface were carried out at the same time. Various ambient gases provided an environment for the device which could change the surface properties by the gas condensing on the surface or reacting chemically with the surface; while chemical treatment provided an exposure of the device surface to either an acidic or an alkaline bath. Depending on the surface conditions, both or either methods might alter the surface layers on the device. However, the gaseous ambient had little if any effect on the surface as evidenced by the I-V characteristics of the devices. Therefore, chemical treatments were used to change the surface layer. Figure 5.9. to Figure 5.12. are families of curves showing the results of the surface treatment sequence.

Some general observation will be given first. The forward I-V characteristics after several surface treatments in NaOH approached ideal diode characteristics. Reverse I-V characteristics improved in the sense that reverse leakage current was reduced until the reverse current is limited by the bulk and "saturates" as shown in Figure 5.10. curves (3) and (4).

As has been stated in 4.3.1., with the termination of valance bonds at the surface, the surface tends to interact with its environment, especially negatively charged ions. As a result, an inversion layer

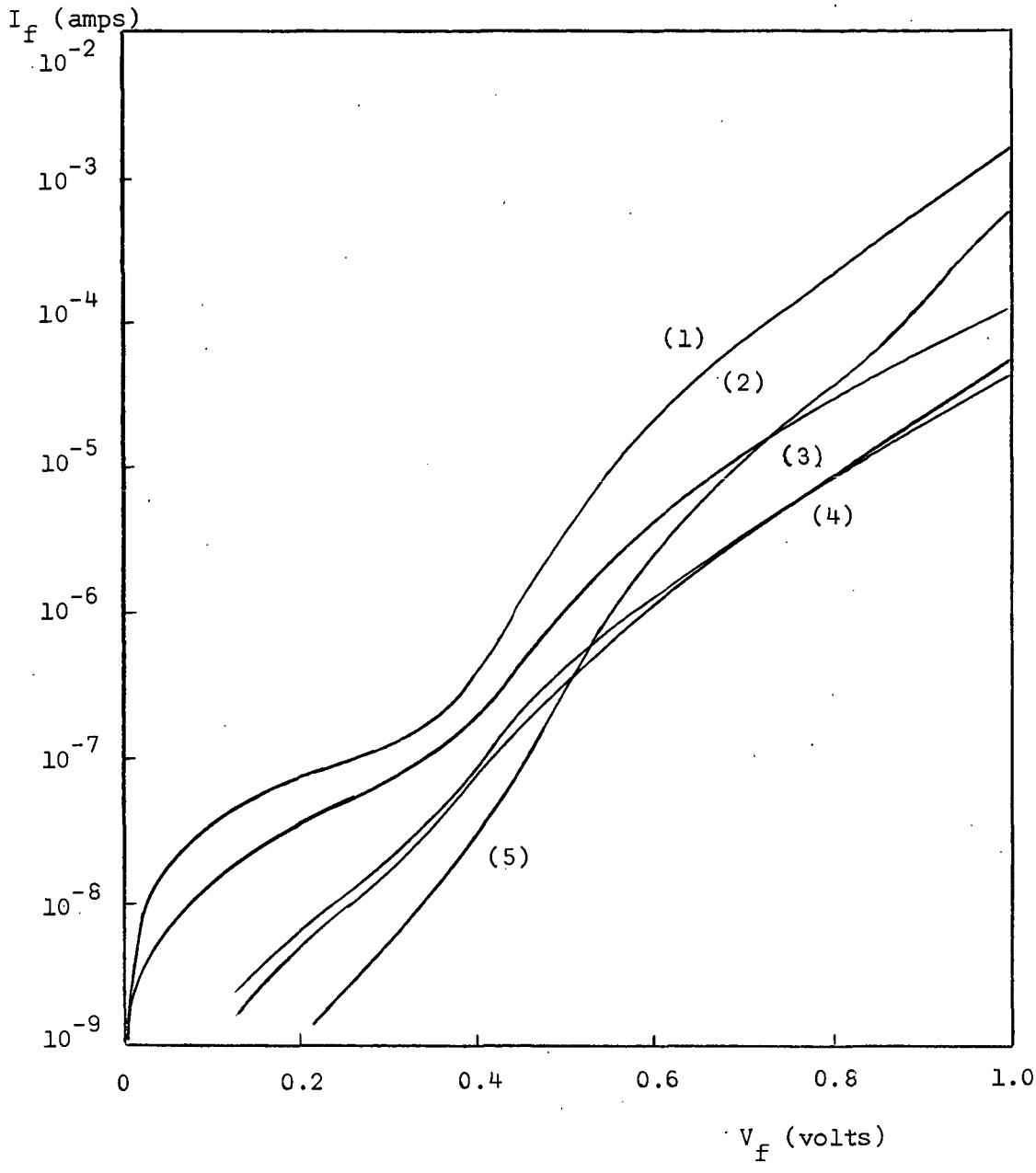


Figure 5.9. Forward I-V characteristic of sample I-E-1 showing surface treatment sequences: (1) before surface treatment (2) after dipping in (5/1) HCl for 58 min. (3) after dipping in (3/1) HCl for another 65 min. (4) after dipping in (2/1) HCl for another 30 min. (5) after switching to (5/1) NaOH and dipping for 120 min.

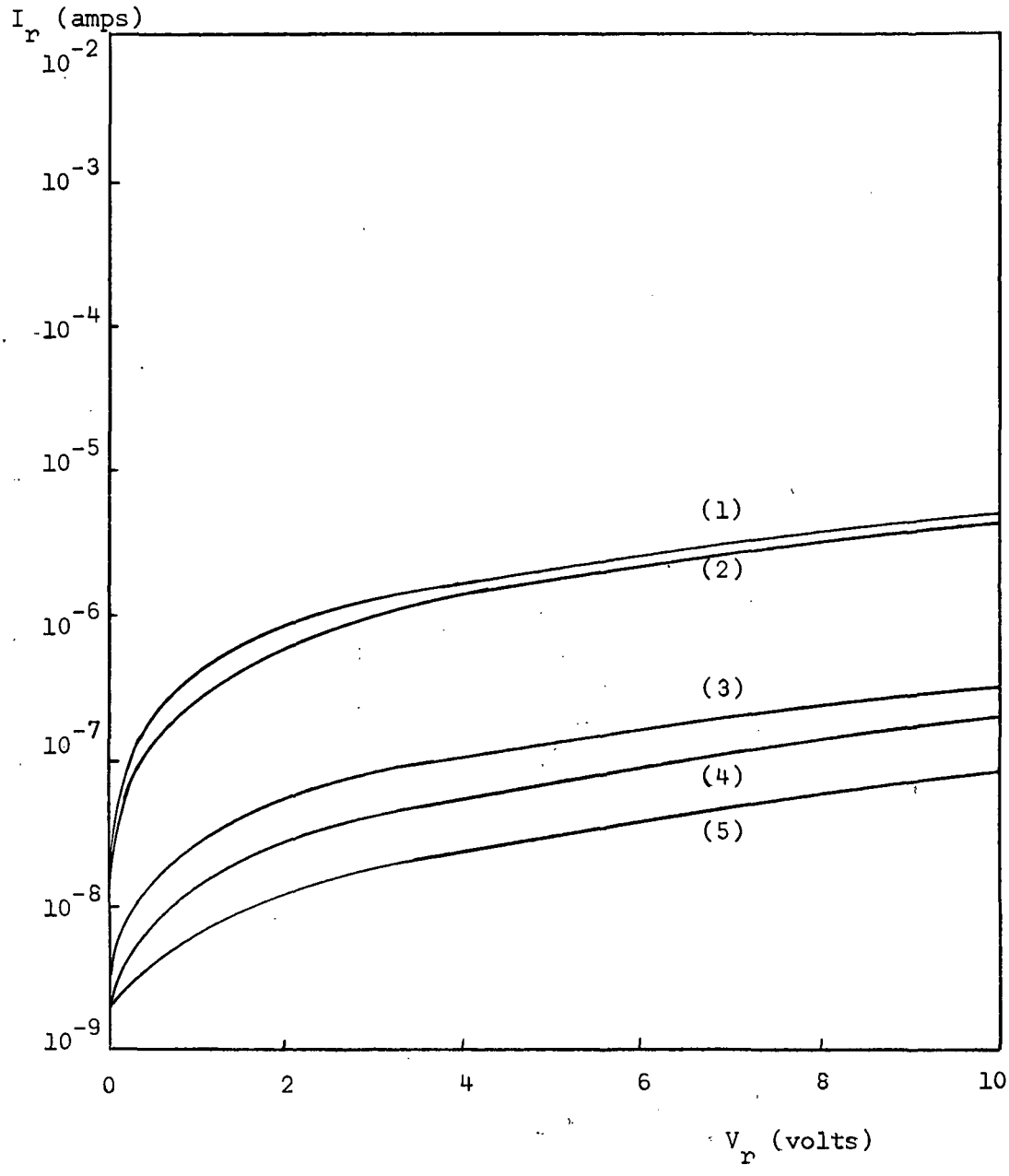


Figure 5.10. Reverse I-V characteristic of sample I-E-1 showing surface treatment sequences: (1) before surface treatment (2) after dipping in (5/1) HCl for 58 min. (3) after dipping in (3/1) HCl for another 65 min. (4) after dipping in (2/1) HCl for another 30 min. (5) after switching to (5/1) NaOH and dipping 120 min.

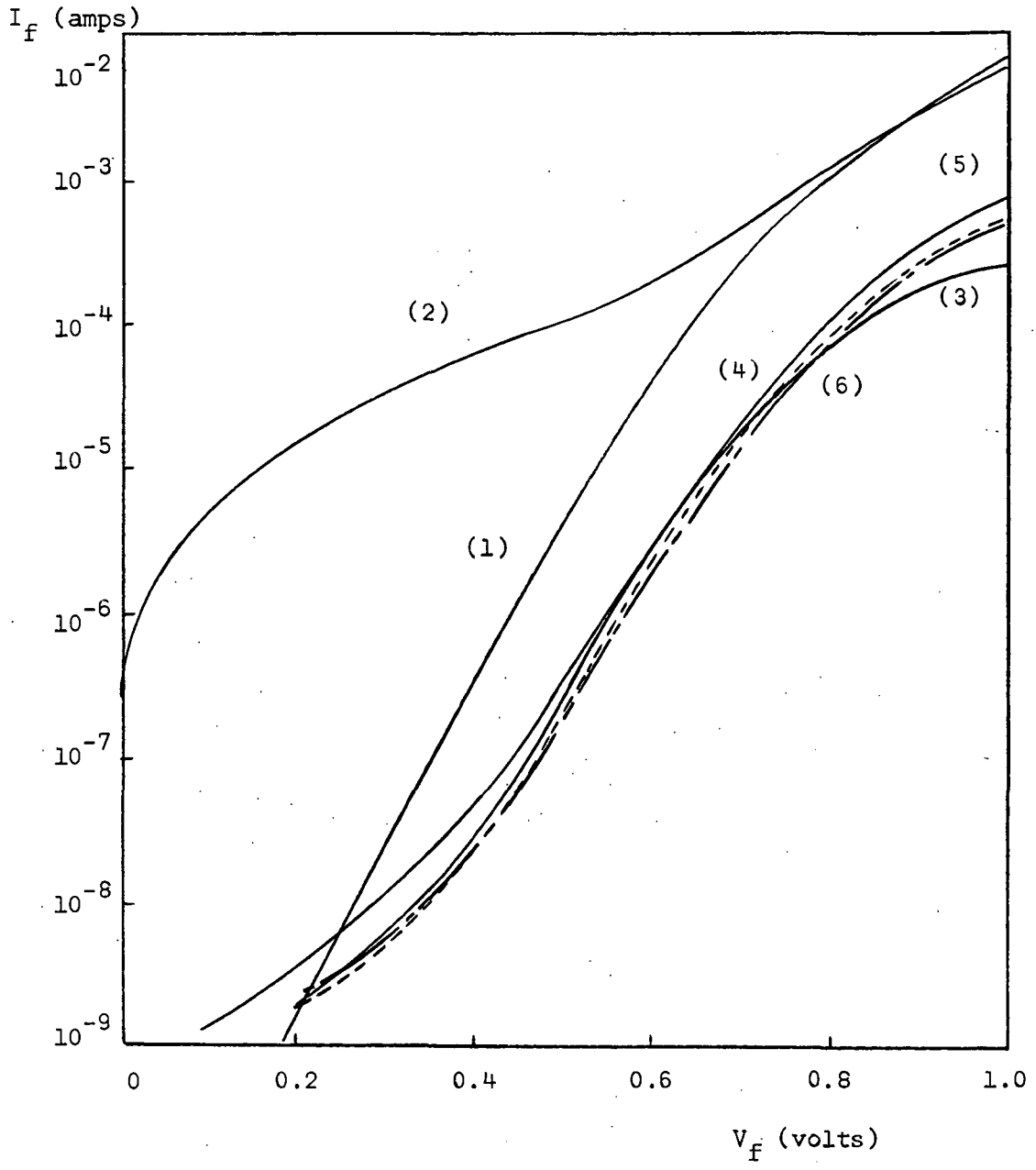


Figure 5.11. Forward I-V characteristics of sample II-E'-1 showing surface treatment sequences: (1) before surface treatment (2) after dipping in (4/1) HCl for 10 min. (3) after dipping in (10/1) NaOH for 10 1/2 min. (4) after dipping in (4/1) HCl for 33 min. (5) after dipping in (5/1) NaOH for 52 min. (6) after dipping in (1/1) HCl for 300 min.

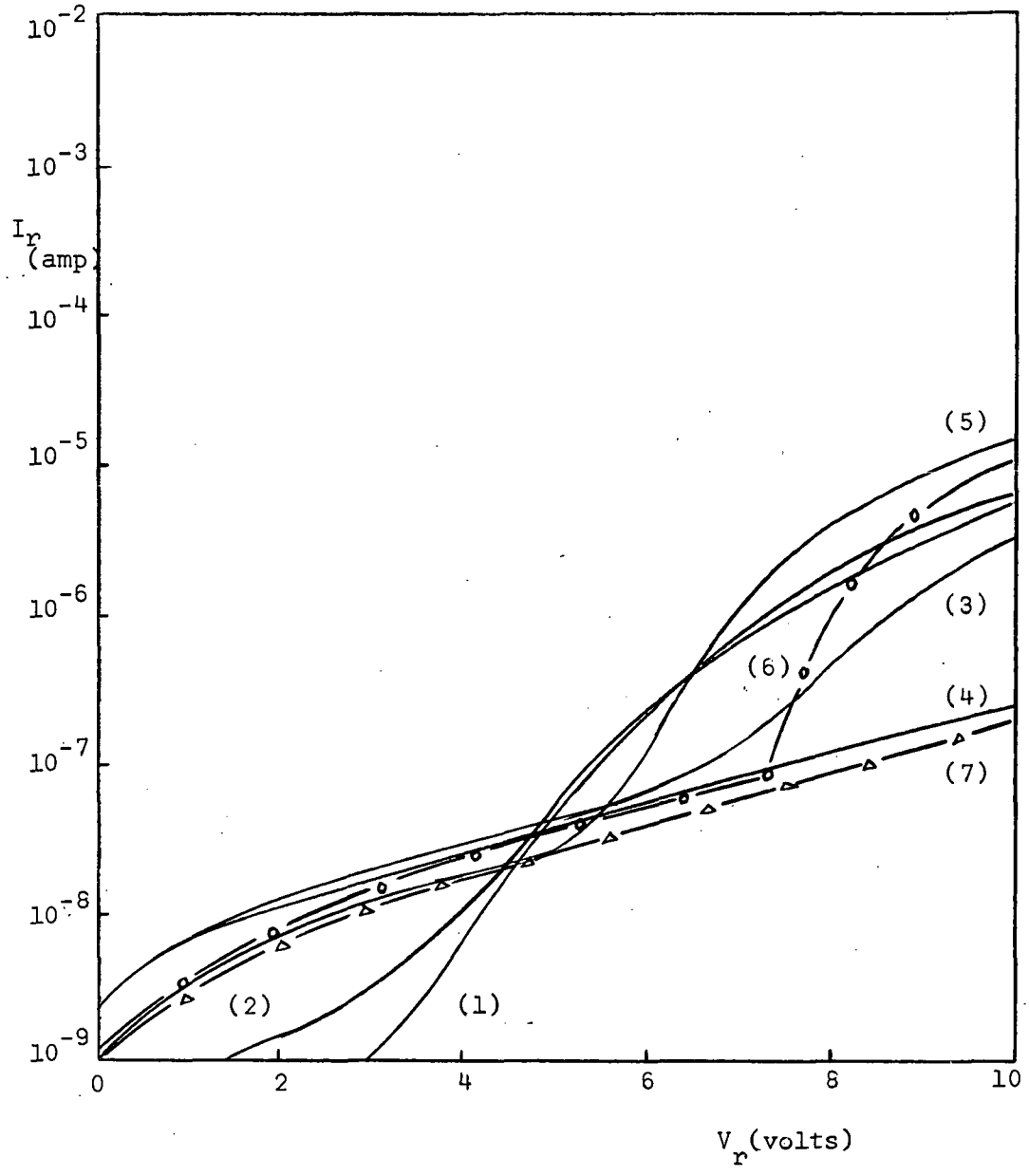


Figure 5.12. Reverse I-V characteristics of sample II-E'-1 showing surface treatment sequences: (1) before surface treatment (2) after dipping in (4/1) HCl for 10 min. (3) after dipping in (10/1) NaOH for 10 1/2 min. (4) after dipping in (4/1) HCl for 33 min. (5) after dipping in (5/1) NaOH for 52 min. (6) after dipping in (1/1) HCl for 300 min. and then (7) another 90 min.

on n-type substrate can be formed immediately underneath the surface. The existence of an inversion layer provides a leakage channel along the surface as shown in Figure 5.13.

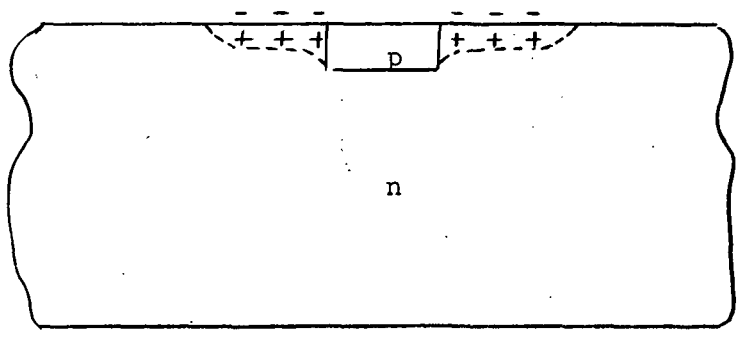


Figure 5.13. The existence of the inversion layer immediately underneath the surface results in the extension of p-region into n-region, thus increasing the conduction area

In the surface treatment, the solutions used were HCl and NaOH respectively. When they are dissolved in deionized water, it is believed that they will give the reactions according to the following formula:

$$HCl \rightleftarrows H^+ + Cl^-$$

$$NaOH \rightleftarrows Na^+ + OH^-$$

By dipping the sample in HCl, the ionic affinity of the surface results in the attachment of Cl^- to the surface. As a result, the inversion layer is enhanced.

With reduction or enhancement of the inversion layer, reverse breakdown of the p-n junction occurs at different values of applied voltage. An explanation can be made using the model proposed by

Garrett et al. (1955) which is reproduced in Figure 5.14. In diagram (a), positive charge resides on the surface of the high resistive n-side of the junction, so the lines of force from these charges will terminate on the ionized acceptors on the p-side. As a result, the field lines will be crowded together at the corner giving rise to the high field there, thus promoting avalanche breakdown. Garrett et al. (1955) made a general observation that surface breakdown, like bulk breakdown, is essentially an avalanche multiplication process. When the surface charge is negative, as shown in diagram (b), the field is lowered at the corner. Now if the surface charge is negative and large, as in diagram (c), the exhaustion region may turn the corner and extend along the surface forming a strong inversion layer which may promote an excess leakage current but will delay surface breakdown until larger reverse voltages are applied. The same model adjusted to the geometry of a planar device is shown in Figure 5.15.

A surface treated by NaOH gives rise to the attachment of positive charges (Na^+) to the surface which tend to reduce the breakdown voltage as shown in Figure 5.12. curves (3) and (5). Figure 5.17. and Figure 5.18. also show this effect. The reverse I-V characteristics for group I samples are shown in Figure 5.10. Breakdown for this group of samples did not occur over the range of measurements.

Breakdown of junctions by whatever mechanism is characterized by a critical field E_c. Fletcher (1957) indicated that, for the case of abrupt junctions, the field under reverse bias conditions could be approximated as shown in Figure 5.16.

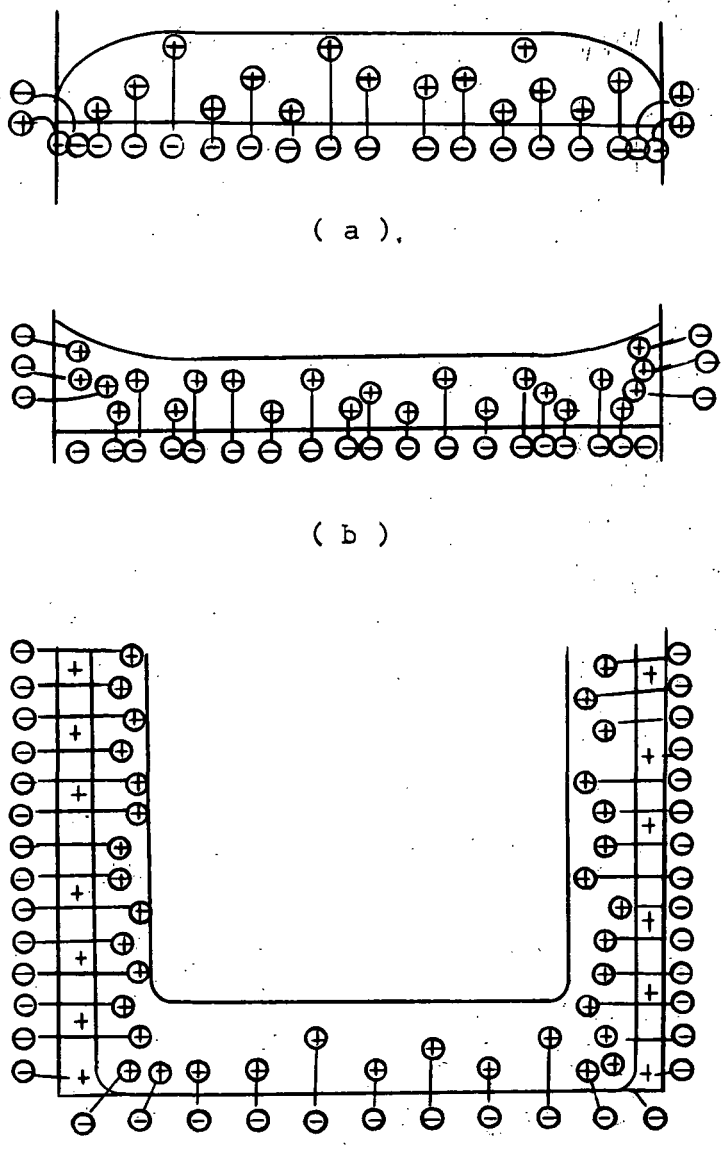


Figure 5.14. Distribution of charge and lines of force with various values for surface charge density σ. (a) σ positive, (b) σ small and negative, (c) σ large and negative. (after Garrett et al. (1955))

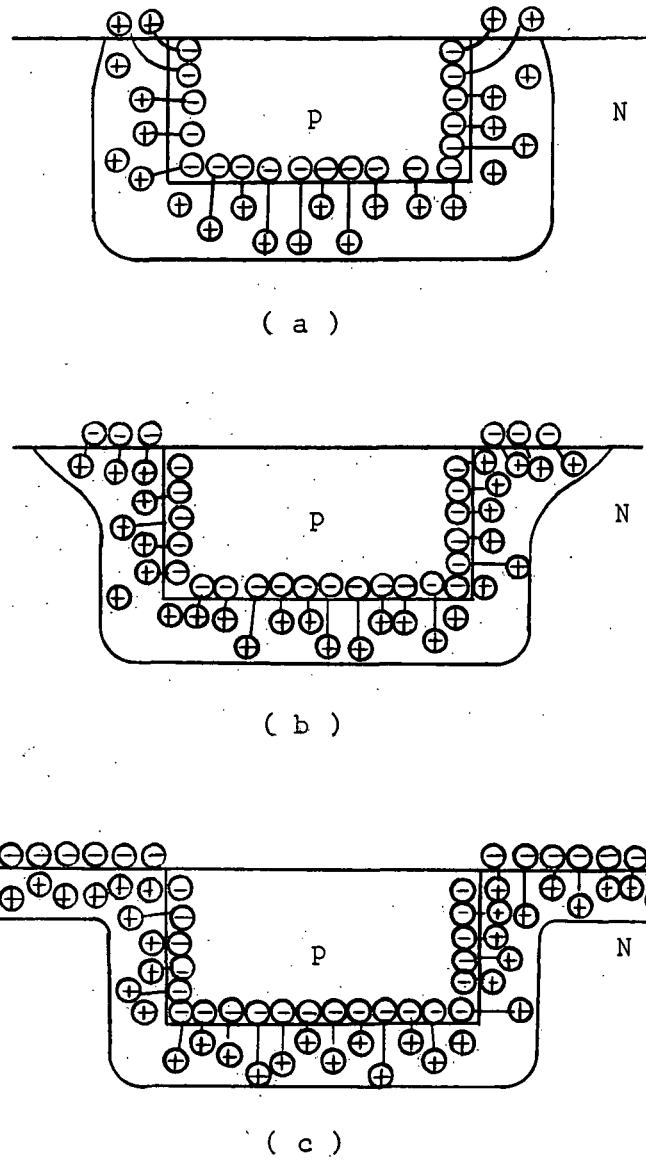


Figure 5.15. Garrett's model of distribution of charges and line of forces fitted into the geometry of the samples used. (a) σ positive, (b) σ small and negative, (c) σ large and negative.

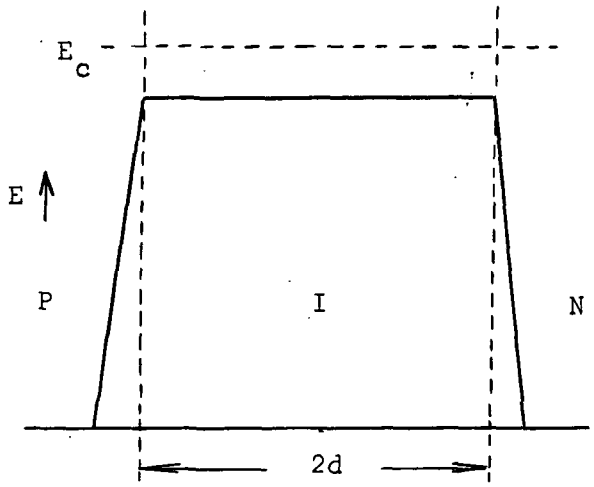


Figure 5.16. Field distribution in reverse-biased p-i-n diode (after Fletcher (1957))

The breakdown voltage across the diode is given by the area under the curve when the applied field is equal to the critical field (E_c) and is approximated by

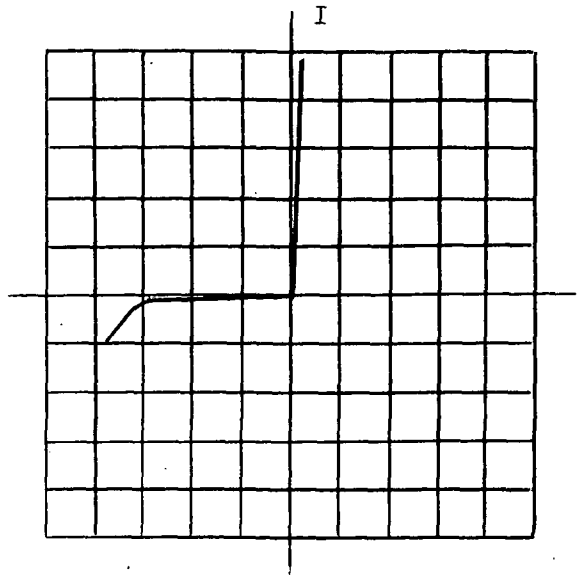
$$V_c = 2\ d\ E_c$$

By assuming E_c = 35 v / μm, and the width of the semi-insulating layer to be 2d = 1.2μm, then

$$V_c = (\ 1.2\ \mu m\ )\ \ (\ 35\ v\ /\ \mu m\ ) = 42\ v$$

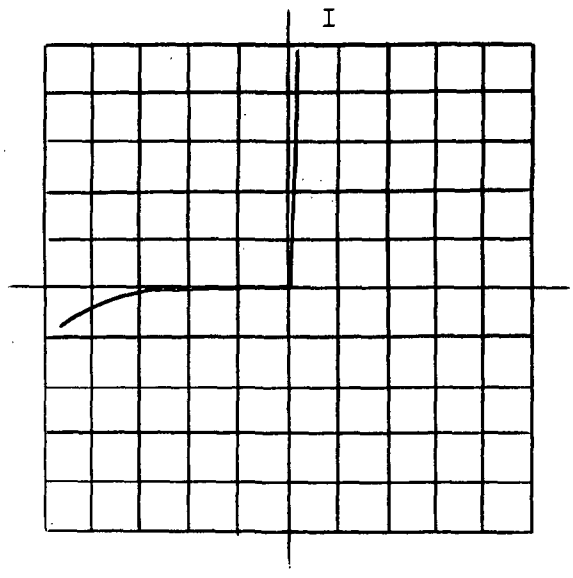
Thus, in theory, the breakdown voltage could be extended to V_r=42 v if the surface breakdown did not take place. However, V_r=42 v is subject to compromise, simply because we assume a true intrinsic region which has a uniform field distribution. In Figure 5.17., it was observed that after surface treatment the breakdown voltage was extended beyond V_r = 30 v which is in close agreement to our estimation.

It thus can be concluded that breakdown voltage as well as the current at low bias, both reverse and forward, were affected by the surface treatment.



(a)

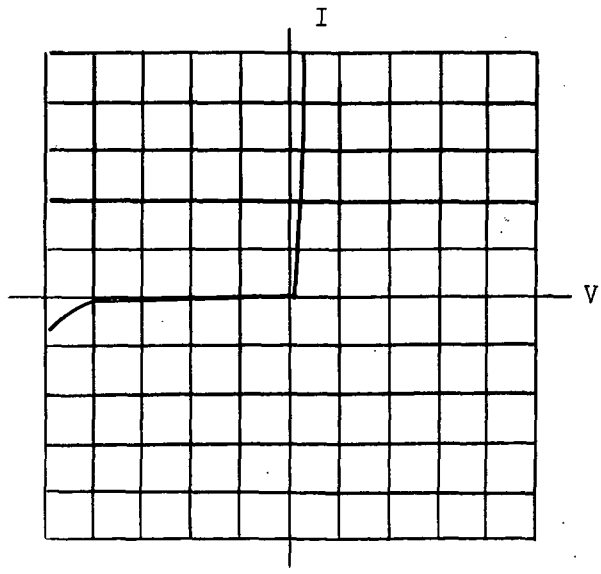
passivated



(b)

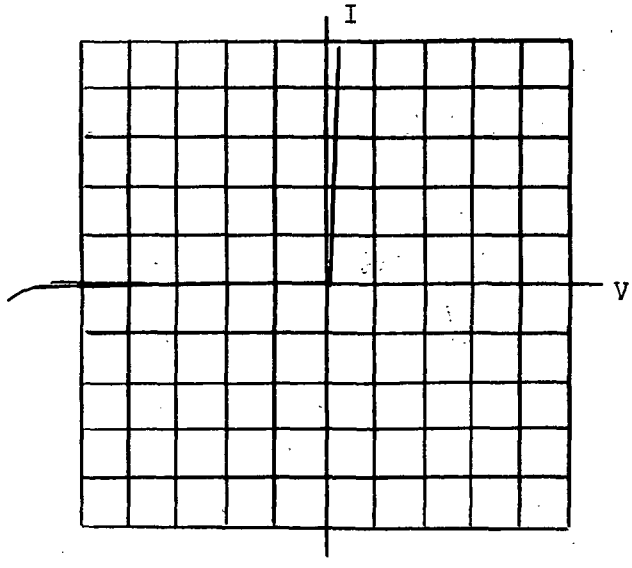
5/l NaOH - 20 min.

Figure 5.17.



(c)

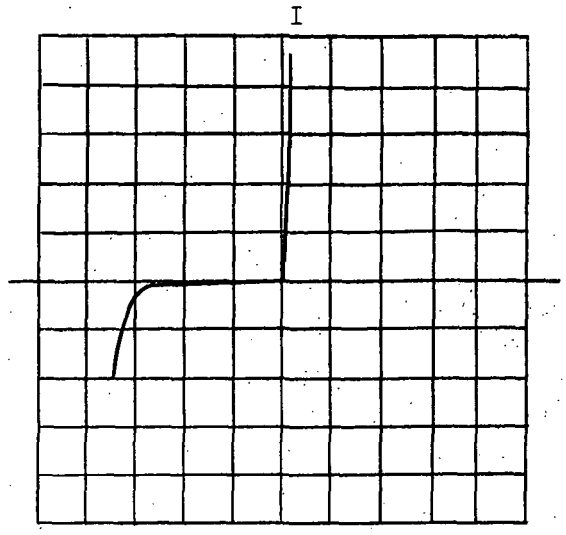
5/1 NaOH - 60 min.



(d)

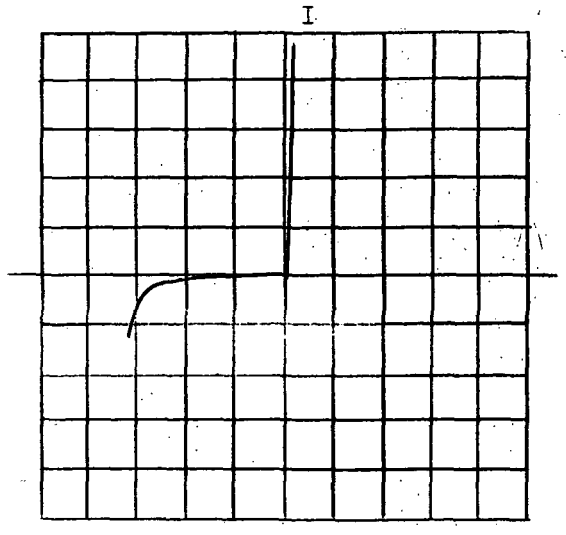
5/1 NaOH - 40 min.

Figure 5.17. I-V characteristics of sample I-E-1 showing surface treatment sequences. The scales are 0.2 ma/div. for I and 5v/div. for V.



(a)

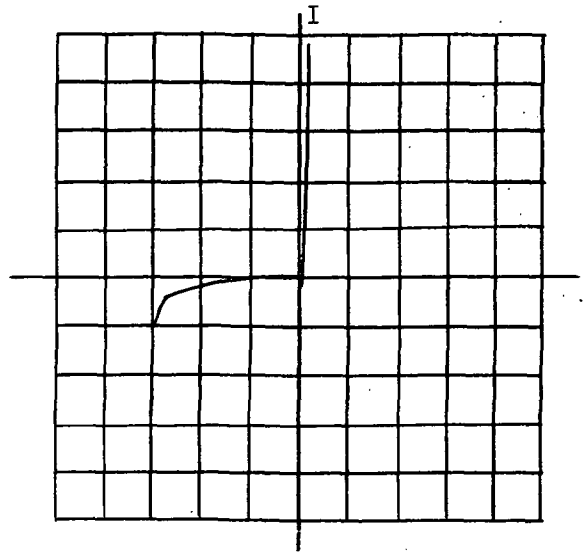
Before Surface treatment



(b)

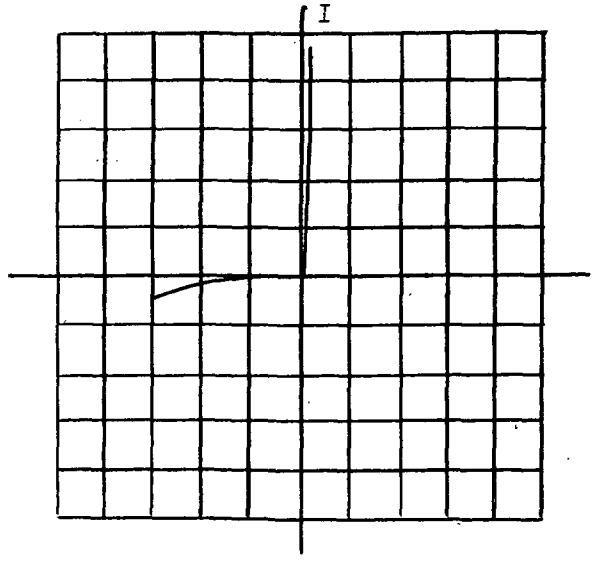
4/1 HCl - 10 min.

Figure 5.18.



(c)

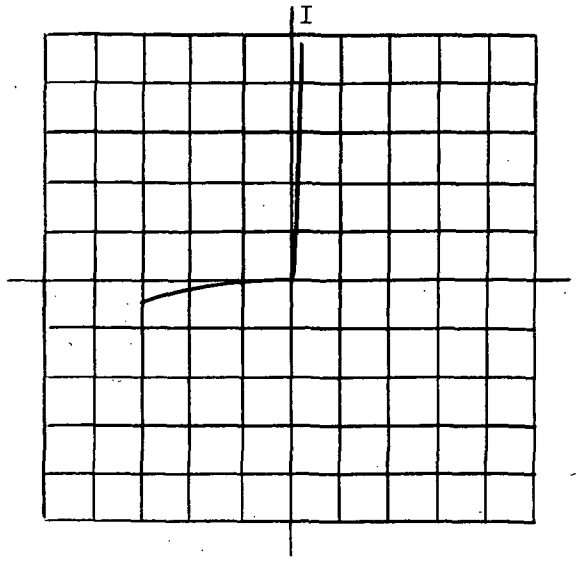
10/1 NaOH - 10 min.



(d)

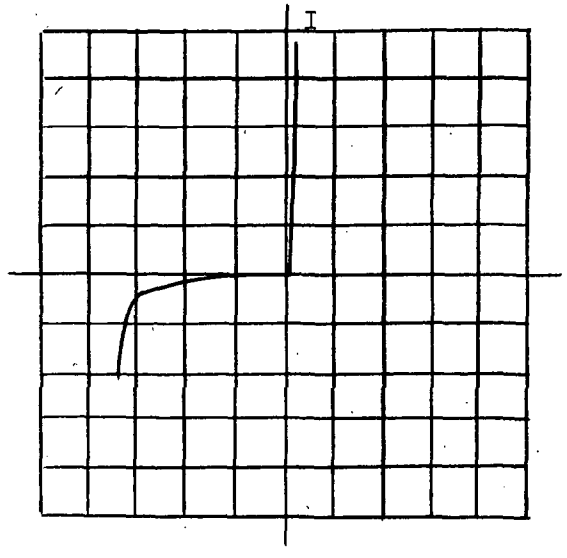
4/1 HCl - 33 min.

Figure 5.18.



(e)

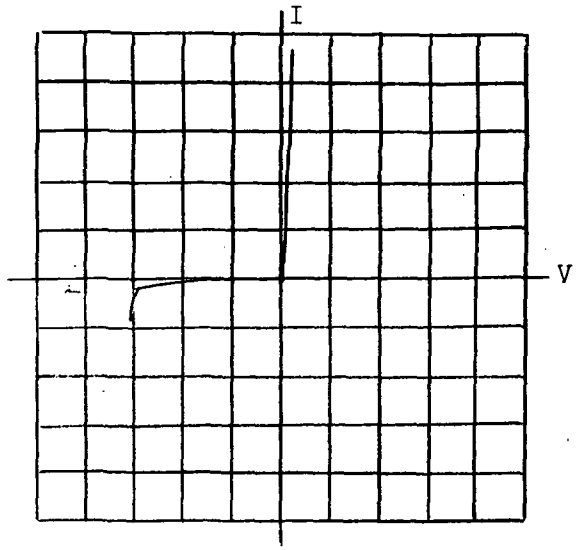
5/l NaOH - 52 min,



(f)

4/l HCl - 300 min.

Figure 5.18.



(g)

1/1 HCl - 90 min.

Figure 5.18. I-V characteristics of sample II-E'-1 showing surface treatment sequences. The scales are 0.2 ma/div. for I and 5v/div. for V.

6. CONCLUSIONS

1. The p-n junctions formed by ion-implanted Zn into n-type GaAs and into n-type (In, Ga)As have been determined by C-V and I-V measurements to be a linearly graded junction.

2. Junctions formed by implanting Zn in (In, Ga)As (group I) are characterized as p-i-n heterojunctions. For group I devices, two parameters which account for observed deviations from ideal diode I-V characteristics are the "mismatch" in the heterojunction and the "thickness" of the intrinsic layer. The junction currents observed are interpreted in terms of Shockley's ideal diode as altered by the heterojunction model proposed by Anderson (1962), the p-i-n diode current model given by Fletcher (1957), and surface leakage currents.

3. As a consequence of an intrinsic layer, generation-recombination current was not observed in group I devices. In contrast, group II devices exhibit a generation-recombination current at low current in both forward and reverse directions. This is evidenced by the fact that the reverse I-V characteristic for group II devices follows a power law while that for group I devices follows an exponential law. Surface leakage currents were more pronounced for group I devices than for group II devices.

4. Surface treatments alter the I-V characteristics of group I and group II devices and the data are repeatable. The reverse breakdown voltage is a sensitive parameter of surface treatment. The mechanism is explainable in terms of inversion layer formation

and ion affinity on the surface. The model of the charge distribution and lines of forces proposed by Garrett et al. (1955) are suitable to interpret the breakdown phenomena and its relationship to the surface treatment.

7. RECOMMENDATION

In order to explore the surface treatment in more depth, and to relate the real surface condition to a more direct parameter and to optimize the surface treatment, it is desirable to develop a method of measuring surface recombination velocity (S). The parameter S is defined by the equation

$$R_s(\Delta n_s) = S\ \Delta n_s \qquad (7.1.)$$

where R_s is the net recombination rate and Δn_s is the excess carrier density at the surface. The concept of surface recombination velocity is related to the lifetime of excess carriers at the surface. $S = 0$ characterizes 'inert' or 'passivated' surface with zero net recombination rate even in the presence of excess carrier densities. $S \to \infty$, on the other hand, implies that the surface does not allow any accumulation of excess carriers which recombine instantly upon arriving at the surface. It is recommended that the measurement of surface recombination velocity be explored for ion-implanted GaAs junctions and the result compared to that in Si and Ge.

8. LIST OF REFERENCES

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9. APPENDICES

9.1 Derivation of Depletion Width on P-N Junctions

9.1.1. Abrupt Junctions

Assume n and p are negligible throughout the space-charge region.

Then, for an abrupt junction

$$N_d - N_a = \begin{cases} -N_a & x<0 \\ N_d & x>0 \end{cases} \qquad (9.1.)$$

where N_a and N_d are constant. For the space-charge region

$$\begin{cases} \nabla^2 V = \frac{q}{\varepsilon} N_a & -d_p \leq x < 0 \\ \nabla^2 V = -\frac{q}{\varepsilon} N_d & 0 < x \leq d_n \end{cases} \qquad (9.2.)$$

Boundary conditions to be satisfied are:

1. V and E constant at x = 0
2. E = 0 when $x = -d_p$ or $x = d_n$.

The solution is

$$V = \frac{q N_a}{\varepsilon} \left(\frac{x^2}{2} + d_p x \right) + C \qquad -d_p \leq x < 0$$

$$V = -\frac{q N_d}{\varepsilon} \left(\frac{x^2}{2} - d_n x \right) + C. \qquad 0 < x \leq d_n$$

(9.3.)

E constant at x = 0 requires that

$$N_a d_p = N_d d_n. \qquad (9.4.)$$

The total depletion region voltage is

$$V_{bi} = V(d_n) - V(-d_p)$$

$$= -\frac{q N_d}{\varepsilon}\left(\frac{d_n^2}{2} - d_n^2\right) + \cancel{C} - \frac{q N_a}{\varepsilon}\left(\frac{d_p^2}{2} - d_p^2\right) - \cancel{C}$$

$$V_{bi} = \frac{q}{2\varepsilon}\left(N_a d_p^2 + N_d d_n^2\right). \qquad (9.5.)$$

Substituting Equation (9.4.) into Equation (9.5.) yields

$$V_{bi} = \frac{q}{2\varepsilon}\left[N_a\left(\frac{N_d}{N_a} d_n\right)^2 + N_d d_n^2\right]$$

$$= \frac{q}{2\varepsilon}\frac{N_d}{N_a}(N_d + N_a) d_n^2$$

or

$$d_n = \left[\frac{2\varepsilon V_{bi}}{q}\frac{N_a}{N_d}\left(\frac{1}{N_d + N_a}\right)\right]^{1/2} \qquad (9.6.)$$

and

$$d_p = \left[\frac{2\varepsilon V_{bi}}{q}\frac{N_d}{N_a}\left(\frac{1}{N_d + N_a}\right)\right]^{1/2}. \qquad (9.7.)$$

Thus, the total depletion width for the abrupt junction is

$$W = d_n + d_p$$

$$= \left[\frac{2\varepsilon}{q} V_{bi}\frac{N_a}{N_d}\left(\frac{1}{N_d + N_a}\right)\right]^{1/2} + \left[\frac{2\varepsilon}{q} V_{bi}\frac{N_d}{N_a}\left(\frac{1}{N_d + N_a}\right)\right]^{1/2}$$

$$= \left[\frac{2\varepsilon}{q} V_{bi}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2} \qquad (9.8.)$$

9.1.2. Linearly Graded Junction

$$N_d - N_a = g\,x \tag{9.9.}$$

where g = constant (cm^{-4}).

Approximations yield the following results:

(a) Using Poisson Equation to solve for V and E

$$\frac{d^2V}{dx^2} = -\frac{q}{\varepsilon}(N_d - N_a) \tag{9.10.}$$

$$= -\frac{q}{\varepsilon}\, g\, x \qquad\qquad -d_p < x < d_n$$

with solutions

$$V = -\frac{q}{\varepsilon}\,\frac{g}{6}x^3 + C_1 x + C_2, \tag{9.11.}$$

$$E = \frac{q}{\varepsilon}\,\frac{g}{2}x^2 - C_1. \tag{9.12.}$$

(b) Using Boltzman relation to solve for V and E for $x > d_n$

$$n(x) \simeq g\,x \qquad\qquad x > d_n \tag{9.13.}$$

$$n(x) = C_1 \exp\left(\frac{q\,V}{k\,T}\right) = g\,x \tag{9.14.}$$

$$\frac{q\,V}{k\,T} = \ln\left(\frac{g}{C_1}\right) x = \ln\, x + C'$$

$$V = \frac{k\,T}{q} \ln x$$

$$E = \frac{k\,T}{q}\,\frac{d\,\ln x}{dx} = \frac{k\,T}{q}\,\frac{1}{x}. \tag{9.15.}$$

(c) Using Boltzman relation to solve for V and E for $x < - d_p$

$$p(x) = - g x \qquad x < - d_p \tag{9.16.}$$

$$E = - \frac{k T}{q} \frac{1}{x}. \tag{9.17.}$$

Maintaining charge neutrality requires

$$\int_{-d_p}^{d_n} (N_d - N_a) \, dx = 0$$

$$\int_{-d_p}^{d_n} g x \, dx = 0$$

$$\frac{g}{2} x^2 \Big|_{-d_p}^{d_n} = 0$$

Therefore,

$$\frac{g}{2} (d_n + d_p)^2 = 0.$$

With

$$\frac{g}{2} \neq 0,$$

requires that

$$|d_n| = |d_p| = d. \tag{9.18.}$$

One of the conditions to be satisfied is E continuous at the boundaries $x = \pm d$.

At $x = - d$

$$\frac{q}{\varepsilon} \frac{g}{2} (-d)^2 - C_1 = \frac{k T}{q} \left(\frac{1}{d} \right)$$

$$C_1 = \frac{q}{\varepsilon}\ \frac{g}{2}(d^2) + \frac{kT}{q}\left(\frac{1}{d}\right).$$

At $x = d$

$$C_1 = \frac{q}{\varepsilon}\ \frac{g}{2}(d^2) + \frac{kT}{q}\left(\frac{1}{d}\right). \qquad (9.19.)$$

Thus solving for V yields

$$V = -\frac{q}{\varepsilon}\ \frac{g}{6}x^3 + C_1 x$$

$$= -\frac{q}{\varepsilon}\ \frac{g}{6}x^3 + \left(\frac{q}{\varepsilon}\frac{g}{2}d^2 + \frac{kT}{q}\frac{1}{d}\right)x.$$

The built-in voltage is obtained from:

$$V_{bi} = V(d_n) - V(-d_p)$$

$$= -\frac{q}{\varepsilon}\frac{g}{6}(d)^3 + \left[\frac{q}{\varepsilon}\frac{g}{2}d^2 + \frac{kT}{q}\ \frac{1}{d}\right]d$$

$$- \left[-\frac{q}{\varepsilon}\frac{g}{6}(-d)^3 + \left[\frac{q}{\varepsilon}\frac{g}{2}d^2 + \frac{kT}{q}\frac{1}{d}\right](-d)\right]$$

$$= \frac{2g}{3}\ \frac{q}{\varepsilon}d^3 + \frac{2kT}{q}.$$

Therefore, we can write

$$\left(V_{bi} - \frac{2kT}{q}\right) = \frac{2g}{3}\frac{q}{\varepsilon}\ d^3 = \frac{q\,g\,W^3}{12\varepsilon} \qquad (9.20.)$$

where $W = 2d$ is the depletion width.

Thus, the depletion width for the linearly graded junctions can be written as

$$W = \left[\frac{12\varepsilon}{qg}\ \left(V_{bi} - \frac{2kT}{q}\right)\right]^{1/3} \qquad (9.21.)$$

9.2. Ideal Current-Voltage Characteristic Equation

Assume

(1) p- and n-type regions are infinitely long

(2) both $I_p = 0$ and $I_n = 0$.

Then, from

$$I_n = 0 = q\, a\, D_n \left(\frac{dn}{dx} + \frac{q\,E}{k\,T}\, n \right) \tag{9.22.}$$

$$I_p = 0 = q\, a\, D_p \left(-\frac{dp}{dx} + \frac{q\,E}{k\,T}\, p \right) \tag{9.23.}$$

and

$$E = -\frac{k\,T}{q}\,\frac{1}{n}\,\frac{dn}{dx} \tag{9.24.}$$

$$E = \frac{K\,T}{q}\,\frac{1}{p}\,\frac{dp}{dx}\,, \tag{9.25.}$$

integrating once yields the total voltage across the junction as

$$V_{bi} - V_a = \frac{k\,T}{q} \ln n \Big|_{\text{p-side}}^{\text{n-side}} = \frac{k\,T}{q} \ln \frac{n_n}{n_p} \tag{9.26.}$$

and

$$V_{bi} - V_a = -\frac{k\,T}{q} \ln p \Big|_{\text{p-side}}^{\text{n-side}} = \frac{k\,T}{q} \ln \frac{p_p}{p_n}\,. \tag{9.27.}$$

In exponential form,

$$n_p = n_n \exp\left(-\frac{q\,V_{bi}}{k\,T}\right) \exp\left(\frac{q\,V_a}{k\,T}\right) = \tilde{n}_p \exp\left(\frac{q\,V_a}{k\,T}\right) \tag{9.28.}$$

and

$$p_n = p_p \exp\left(-\frac{q V_{bi}}{k T}\right) \exp\left(\frac{q V_a}{k T}\right) = \bar{p}_n \exp\left(\frac{q V_a}{k T}\right), \qquad (9.29.)$$

where

$$\bar{n}_p = n_n \exp\left(-\frac{q V_{bi}}{k T}\right) \qquad (9.30.)$$

$$\bar{p}_n = p_p \exp\left(-\frac{q V_{bi}}{k T}\right)$$

are thermal equilibrium concentrations.

Since the lifetime of the injected carriers is finite, the above equations (Eq. 9.28. and 9.29.) are not strictly correct. However, for low current, little error is introduced by assumptions. Rewrite,

$$n_{p0} = \bar{n}_{p0} \exp\left(\frac{q V}{k T}\right) \qquad (9.31.)$$

$$p_{n0} = \bar{p}_{n0} \exp\left(\frac{q V}{k T}\right) \qquad (9.32.)$$

where "0" stands for depletion region boundaries.

The loss of hole current due to recombination is expressed in terms of the recombination rate $\hat{p} / \tau_p$ as

$$d I_p = - q a \, dx \frac{\hat{p}}{\tau_p} \qquad (9.33.)$$

or

$$\frac{d I_p}{d x} = - q a \frac{\hat{p}}{\tau_p} . \qquad (9.34.)$$

But

$$I_p \text{ (diffusion)} = - q\, a\, D_p \frac{dp}{dx} \tag{9.35.}$$

and (9.34.) can be written as

$$D_p \frac{d^2 p}{dx^2} = \frac{\hat{p}}{\tau_p} . \tag{9.36.}$$

Since

$$p = \bar{p} + \hat{p} \tag{9.37.}$$

we can write

$$\frac{d^2 p}{dx^2} = \cancel{\frac{d^2 \bar{p}}{dx^2}}^{\,0} + \frac{d^2 \hat{p}}{dx^2} = \frac{\hat{p}}{D_p \tau_p} \tag{9.38.}$$

where p is invariant with distance.

The solution is

$$\hat{p} = C_1 \exp\left(- \frac{x}{\sqrt{D_p \tau_p}}\right) + C_2 \exp\left(\frac{x}{\sqrt{D_p \tau_p}}\right). \tag{9.39.}$$

Boundary conditions to be satisfied are

$$\hat{p} \to 0 \quad \text{as } x \to \infty \quad \text{thus } C_2 = 0$$

$$\hat{p} \to P_0 \quad \text{at } x = 0 \quad \text{thus } C_1 = \hat{P}_0 .$$

Therefore, we obtain

$$\hat{p} = \hat{P}_0 \exp\left(- \frac{x}{\sqrt{D_p \tau_p}}\right) = \hat{P}_0 \exp\left(- \frac{x}{L_p}\right) \tag{9.40.}$$

where L_p is defined as the diffusion length.

The current flowing is the sum of the hole and electron currents at any point along the semiconductor. However, it is more convenient to take the sum at the junction, where the current is already known. It is also noted that the hole current entering the n-region is determined by

the slope of the excess hole concentration at the junction.

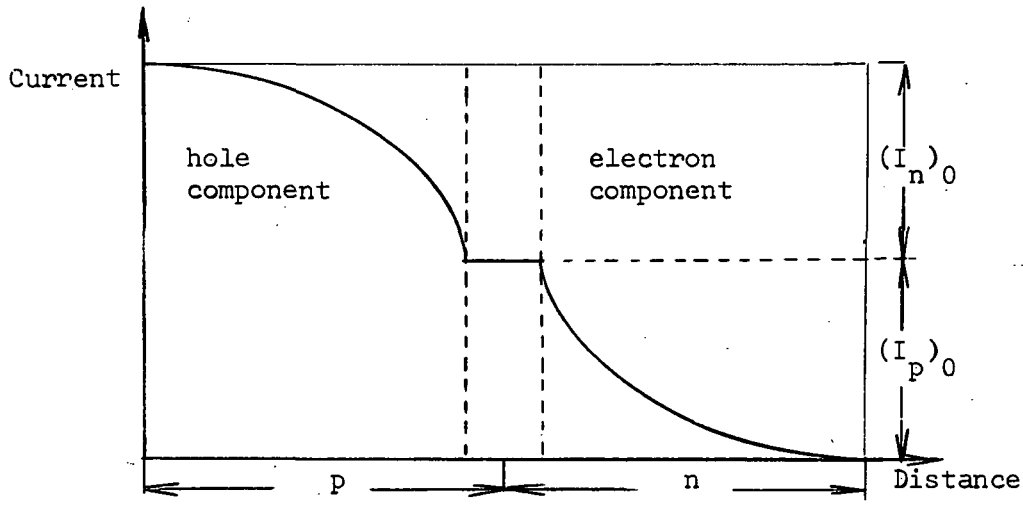

Figure 9.1. Current variations with distance across the junction

$$I_p = - q\, a\, D_p \left.\frac{d\hat{p}}{dx}\right|_{junction} = q\, a \left(\frac{D_p}{\tau_p}\right)^{1/2} \hat{p}_0 \qquad (9.41.)$$

$$I_n = q\, a\, D_n \left.\frac{d\hat{n}}{dx}\right|_{junction} = q\, a \left(\frac{D_n}{\tau_n}\right)^{1/2} \hat{n}_0 \qquad (9.42.)$$

$$I = I_p + I_n$$

$$= q\, a \left[\left(\frac{D_p}{\tau_p}\right)^{1/2} \hat{p}_0 + \left(\frac{D_n}{\tau_n}\right)^{1/2} \hat{n}_0 \right] \qquad (9.43.)$$

or

$$I = q\, a \left[\left(\frac{\hat{p}_0}{\tau_p}\right) L_p + \left(\frac{\hat{n}_0}{\tau_n}\right) L_n \right] \qquad (9.44.)$$

and

$$n_{p0} = \bar{n}_{p0} + \hat{n}_0$$

$$p_{n0} = \bar{p}_{n0} + \hat{p}_0 \,.$$

Therefore,

$$\hat{n}_0 = n_{p0} - \bar{n}_{p0}$$

$$\hat{p}_0 = p_{n0} - \bar{p}_{n0}$$

$$\hat{n}_0 = \bar{n}_{p0} \exp\left(\frac{q V_a}{k T}\right) - \bar{n}_{p0}$$

$$= \bar{n}_{p0}\left[\exp\left(\frac{q V_a}{k T}\right) - 1\right] \qquad (9.45.)$$

Likewise,

$$\hat{p}_0 = \bar{p}_{n0}\left[\exp\left(\frac{q V_a}{k T}\right) - 1\right] . \qquad (9.46.)$$

Substituting (9.45.) and (9.46.) into (9.43.) we get,

$$I = q\, a\left[\exp\left(\frac{q V_a}{k T}\right) - 1\right]\left[\left(\frac{D_p}{\tau_p}\right)^{1/2} \bar{p}_{n0} + \left(\frac{D_n}{\tau_n}\right)^{1/2} \bar{n}_{p0}\right] \qquad (9.47.)$$

and substituting into (9.44.) we get,

$$I = q\, a\left[\exp\left(\frac{q V_a}{k T}\right) - 1\right]\left[\left(\frac{\bar{p}_{n0}}{\tau_p}\right) L_p + \left(\frac{\bar{n}_{p0}}{\tau_n}\right) L_n\right]$$

$$= I_s\left[\exp\left(\frac{q V_a}{k T}\right) - 1\right] \qquad (9.48.)$$

where

$$I_s = q\, a\left[\left(\frac{\bar{p}_{n0}}{\tau_p}\right) L_p + \left(\frac{\bar{n}_{p0}}{\tau_n}\right) L_n\right] . \qquad (9.49.)$$

9.3. Avalanche Breakdown

Assume:

(1) The depletion layer is free from recombination.

(2) No additional space charge effects from the carriers produced by ionization.

Define:

(1) The ionization rate $a_i(E)$ as the number of electron-hole pairs being generated per unit distance by a single electron moving in the x direction.

(2) The multiplication factor M as the ratio of the number of electrons leaving at x_n to the number of electrons entering at x_p.

$$M = n / n_0$$

Denote:

n_0: the number of electrons entering at $x = x_p$ per unit time

n : the number of electrons entering at $x = x_n$ per unit time

n_1: the number of electrons generated per unit time between x and x_p

n_2: the number of electrons generated per unit time between $x + dx$ and x_n

dn_1: the number of electrons generated per unit time between x and $x + dx$

Then,

$$dn_1 = (n_0 + n_1) a_i \, dx + n_2 a_i \, dx = n a_i \, dx \quad (9.50.)$$

$(n_0 + n_1) a_i \, dx$: Number of electron-hole pairs generated by electron coming from the left

$n_2 a_i \, dx$: same from the right

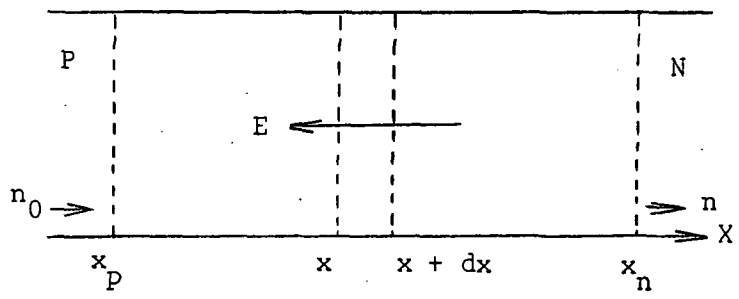

Figure 9.2. Schematic diagram showing the number of electrons at various points along x direction

where

$$n = n_0 + n_1 + n_2$$

The multiplication factor is defined as

$$M = n / n_0 \tag{9.51.}$$

Since the number of electrons generated by ionization in the space charge region between x_p and x_n per unit time is given by

$$\int_{x_p}^{x_n} dn_1 = n - n_0 = n \int_{x_p}^{x_n} a_i \, dx \tag{9.52.}$$

the multiplication factor becomes

$$M = \frac{n}{n_0} = \frac{1}{1 - \int_{x_p}^{x_n} a_i \, dx} \tag{9.53.}$$

9.4. Rough Estimation of Depletion Layer Thickness

The diameter of the junction area is given as

$$D = 40 \text{ mil}$$

and the area is

$$a = 40 \times 10^{-3} \times 2.54 \times 3.14 = 0.319 \text{ cm}^2.$$

The capacitance can be expressed as

$$C = \frac{\varepsilon a}{d}$$

where

$$\varepsilon = 12 \times 8.854 \times 10^{-14} \quad \text{Farad / cm}$$

$C_0 = 318.4$ pf (capacitance at 0 v bias)

$C_{10} = 148.7$ pf (capacitance at 10 v bias).

Therefore, the depletion layer thickness can be calculated as

$$d_0 = \frac{0.319(\text{cm}^2) \times 12 \times 8.854 \times 10^{-14} \text{ (Farad/cm)}}{320 \times 10^{-12} \text{ (Farad)}}$$

$$= 10 \text{ microns}$$

$$d_{10} = \frac{0.319 \times 12 \times 8.854 \times 10^{-14}}{150 \times 10^{-12}}$$

$$= 22.6 \text{ microns.}$$

9.5. List of Symbols

a	cross-sectional area of p - n junction
C	capacitance
D_n	diffusion coefficient of electrons
D_p	diffusion coefficient of holes
d_n	depletion length of n type material
d_p	depletion length of p type material
E	electric field
E	electron energy
E_c	electron energy at conduction band edge
E_g	width of forbidden gap energy
E_v	electron energy at valence band edge
E_f	electron energy at the Fermi level
ε	dielectric constant (relative permitivity of the material)
g	the impurity concentration gradient at the junction in cm^{-4}
K	Boltzmann's constant 8.62×10^{-5} ev/°k
I_s	diffusion current in neutral region
I_g	generation current in depletion region
L_n	diffusion length of electrons
L_p	diffusion length of holes
M	avalanche multiplication factor
M_1	arbitrary constant
M_2	arbitrary constant
m^*	effective mass
N_a	acceptor impurity concentration
N_d	donor impurity concentration

n electron concentration (cm^{-3})

n_i intrinsic carrier concentration

n_n electron concentration in an n-type region

$\bar{n}_p$ electron concentration in equilibrium in p-type material

n_p electron concentration in p region

$\hat{n}$ excess electron carrier concentration (cm^{-3})

p hole concentration

p_p hole concentration in a p-type semiconductor (majority carrier concentration)

p_n hole concentration in an n-type region

$\hat{p}$ excess hole carrier concentration (cm^{-3})

ρ space-charge density

Q total charge

q magnitude of electronic charge, 1.6×10^{-19} coulomb

R recombination rate (per unit time per unit volume)

S surface recombination velocity

T Temperature

τ decay time

V Voltage

V_a Applied bias voltage

V_{bi} built-in voltage at the junction

v_{b1} built-in voltage supported by material 1 in heterojunction

V_{b2} built-in voltage supported by material 2 in heterojunction

V_d total voltage appearing at the heterojunction

V_F forward bias voltage

V_R reverse bias voltage

W total depletion width

X transmission coefficient for heterojunction